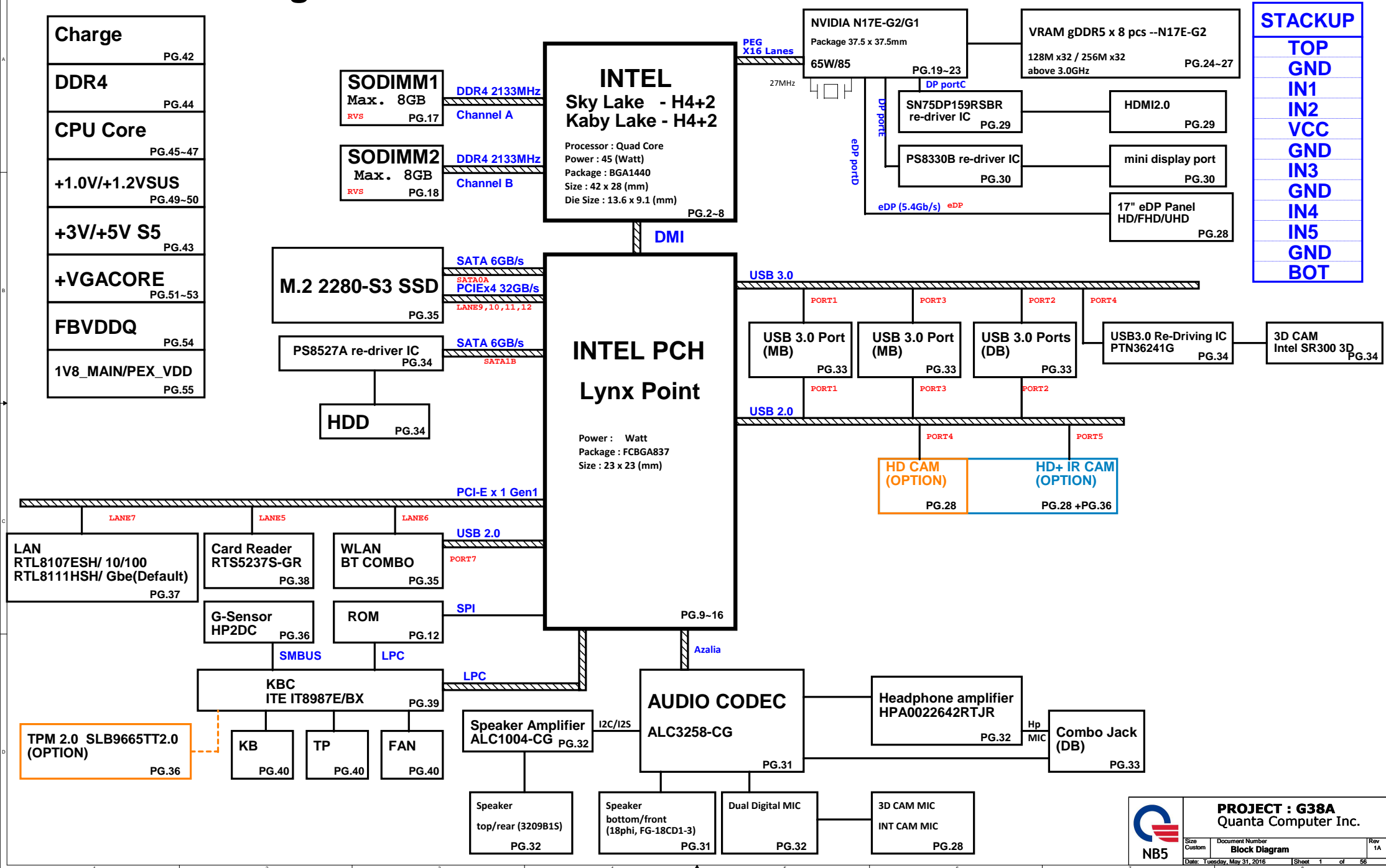


Pavilion Gaming Griffin1.1 INTEL SKL / KABY -H SYSTEM DIAGRAM

01



H_PROCHOT# R3 1K 4 1.0V

XDP_TDO_CPU R5 51 4 1.0V

XDP_TMS_CPU R6 51 4


XDP_TDI_CPU R7 51 4

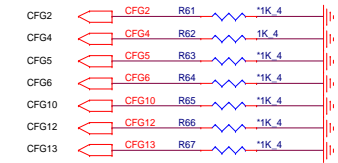
XDP_PREQ# R8 51 4

XDP_TRST#_CPU R10 51 4

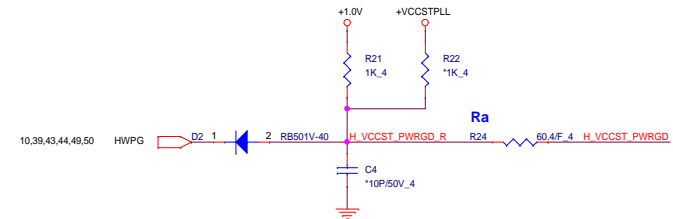
XDP_TRST# R12 51 4

The CFG signals have a default value of '1' if not terminated on the board.

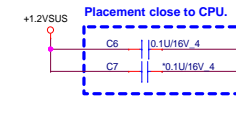
CFG3 



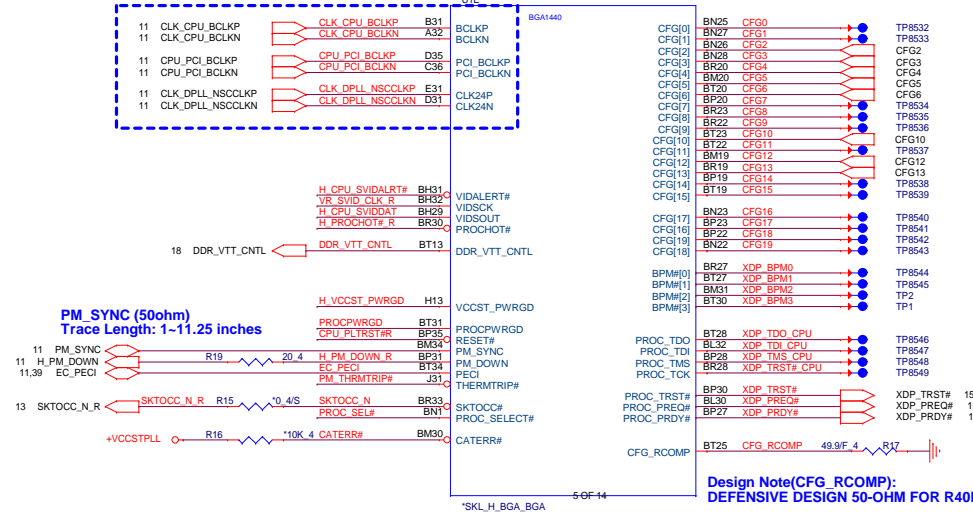
Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



Note: please keep plane is enough for VDDQ 2.8A



Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impedence 85 ohm

[illegible]

11 CPU_PLTRST#

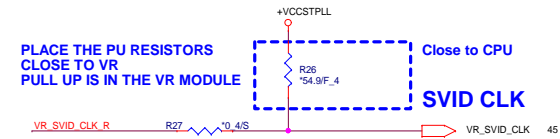
12,19,35,36,37,38,39 PLTRST#

R11 1.5K_F_4

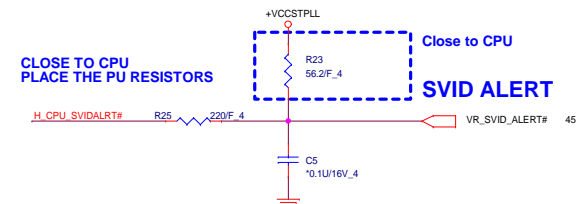
R13 750F_F_4

CPU_PLTRST#

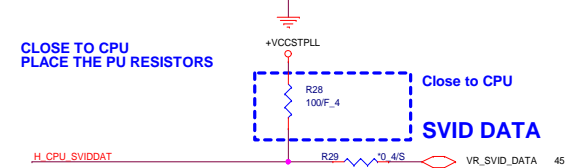
SVID CLK



SVID ALERT



SVID DATA



5.11.39 PM_THRMTRIP#

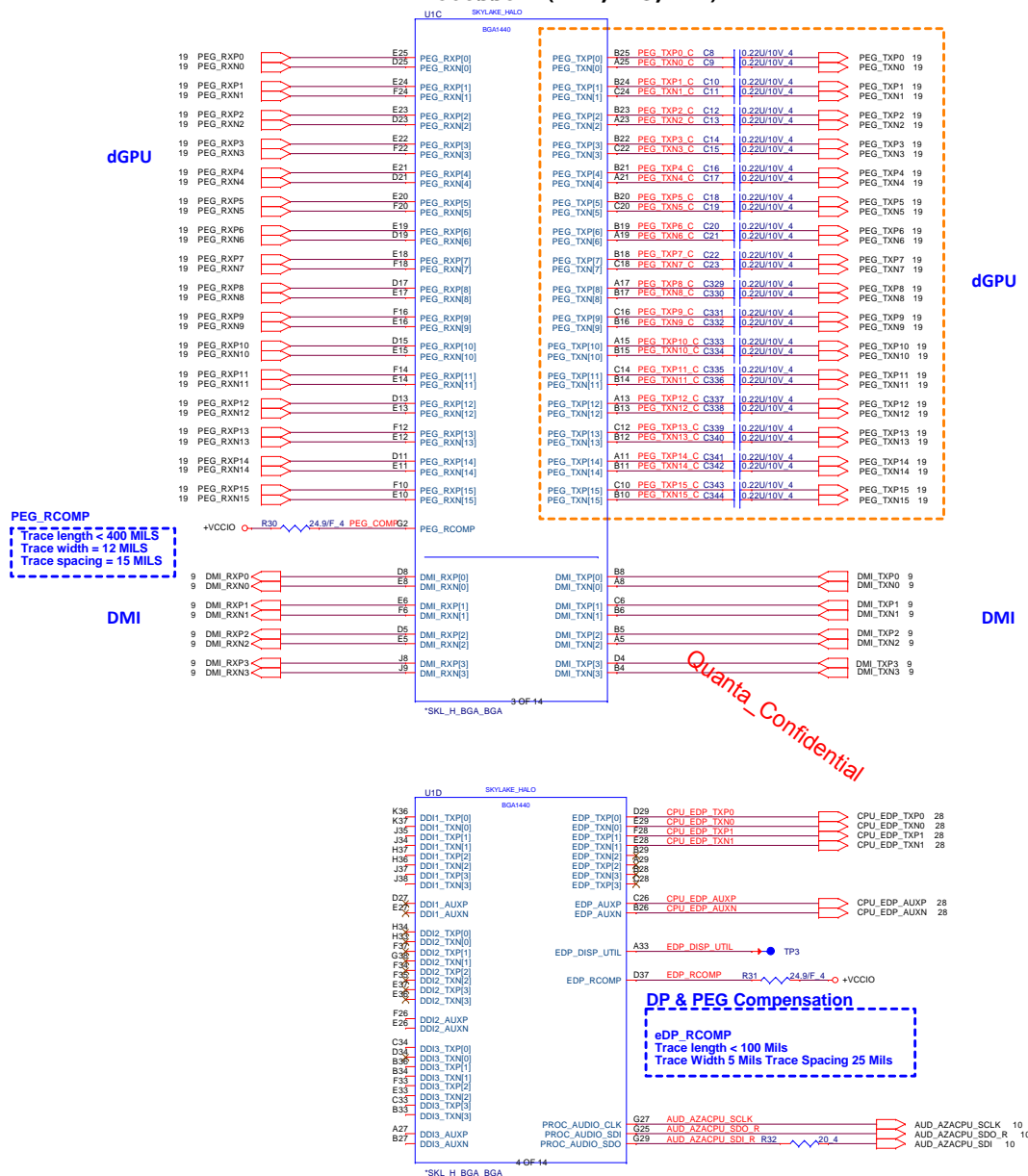
Rb

+VCCSTPLL

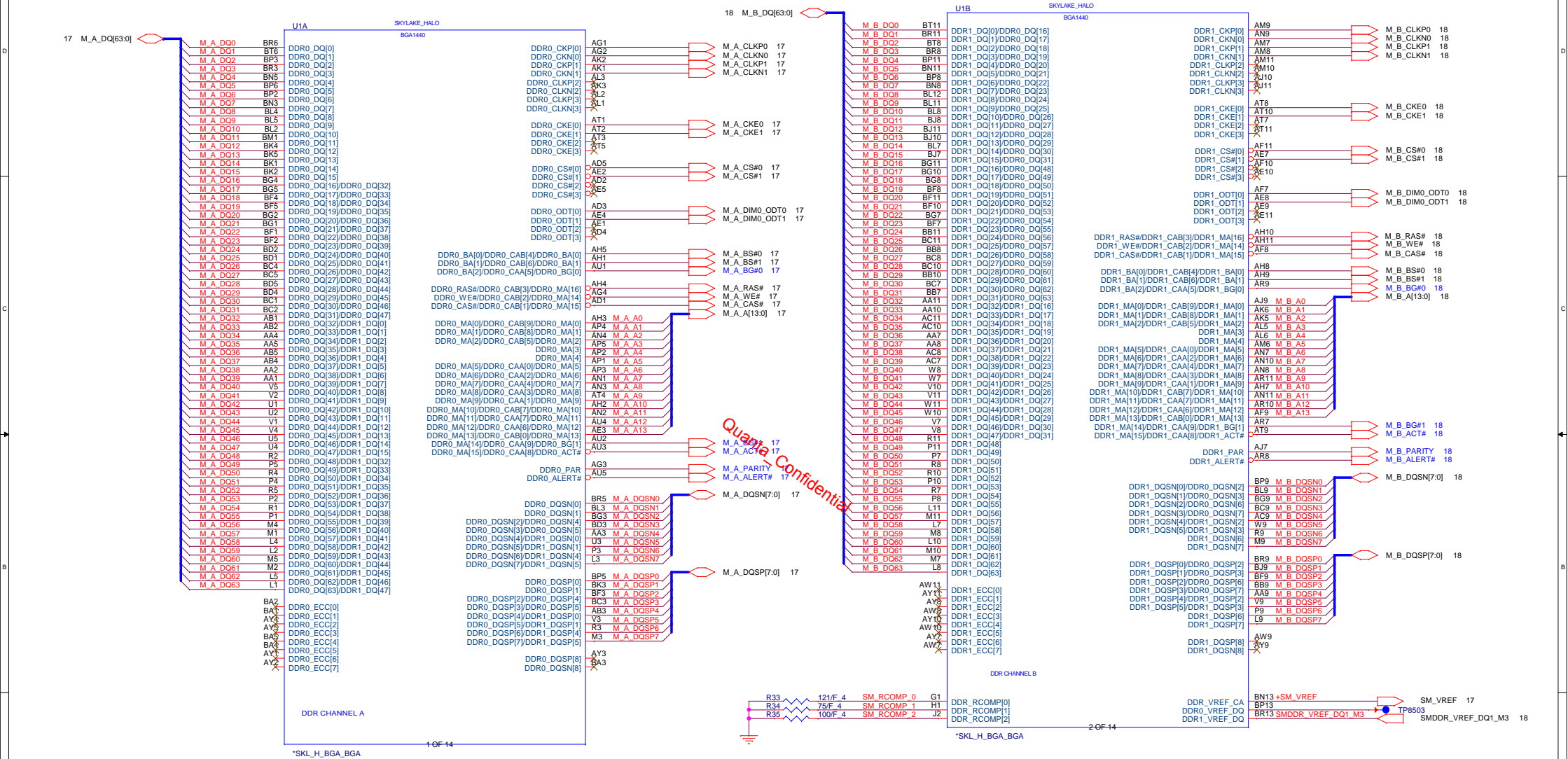
R14 1K 4

PM_THRMTRIP#

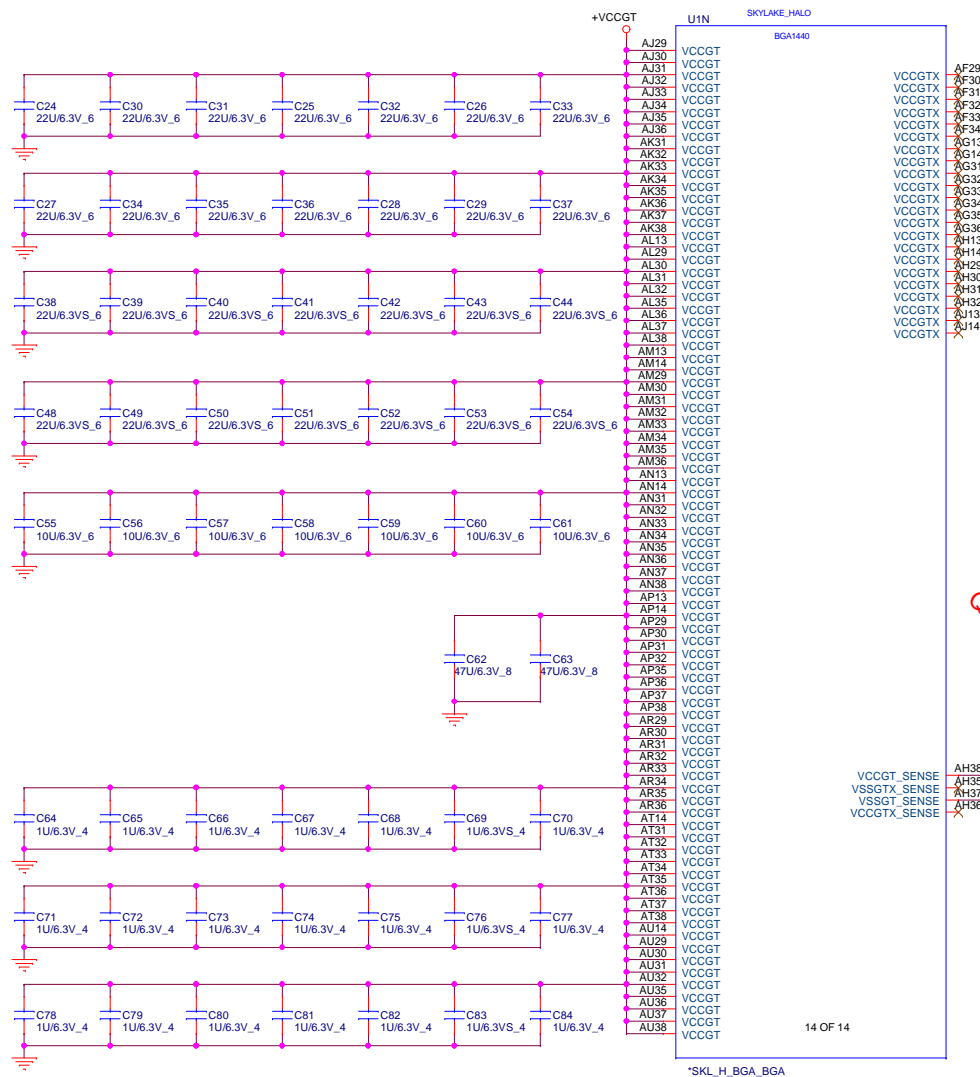
SKYLAKE Processor (DMI, PEG, FDI)



SKYLAKE Processor (DDR4)



Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A



Quanta_Confidential

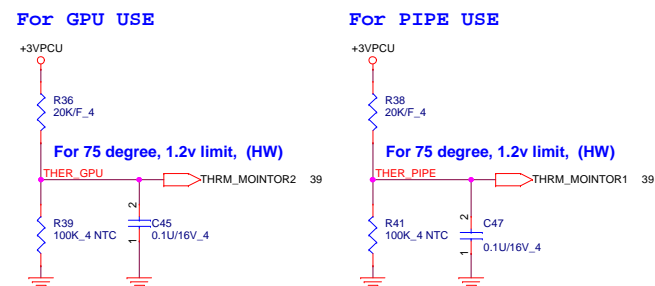
14 OF 14

*SKL H BGA BGA



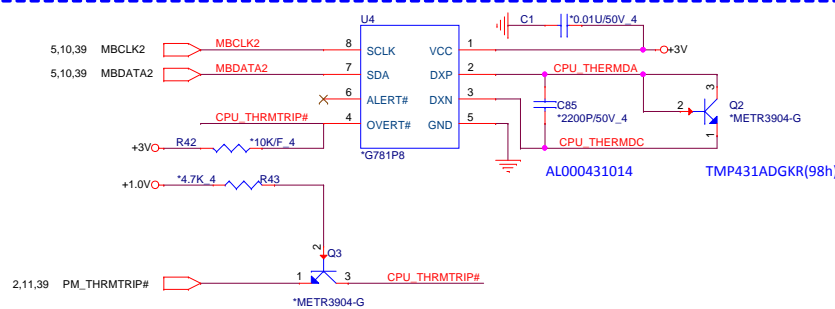
IO Thrm Protect

Location need thermal confirm

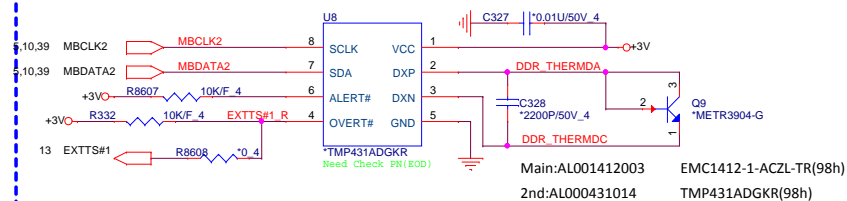


CPU Thermal Sensor

Location need thermal confirm



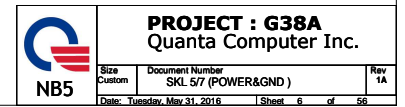
GPU Thermal Sensor



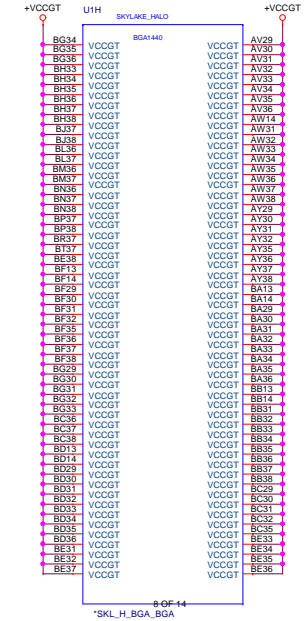
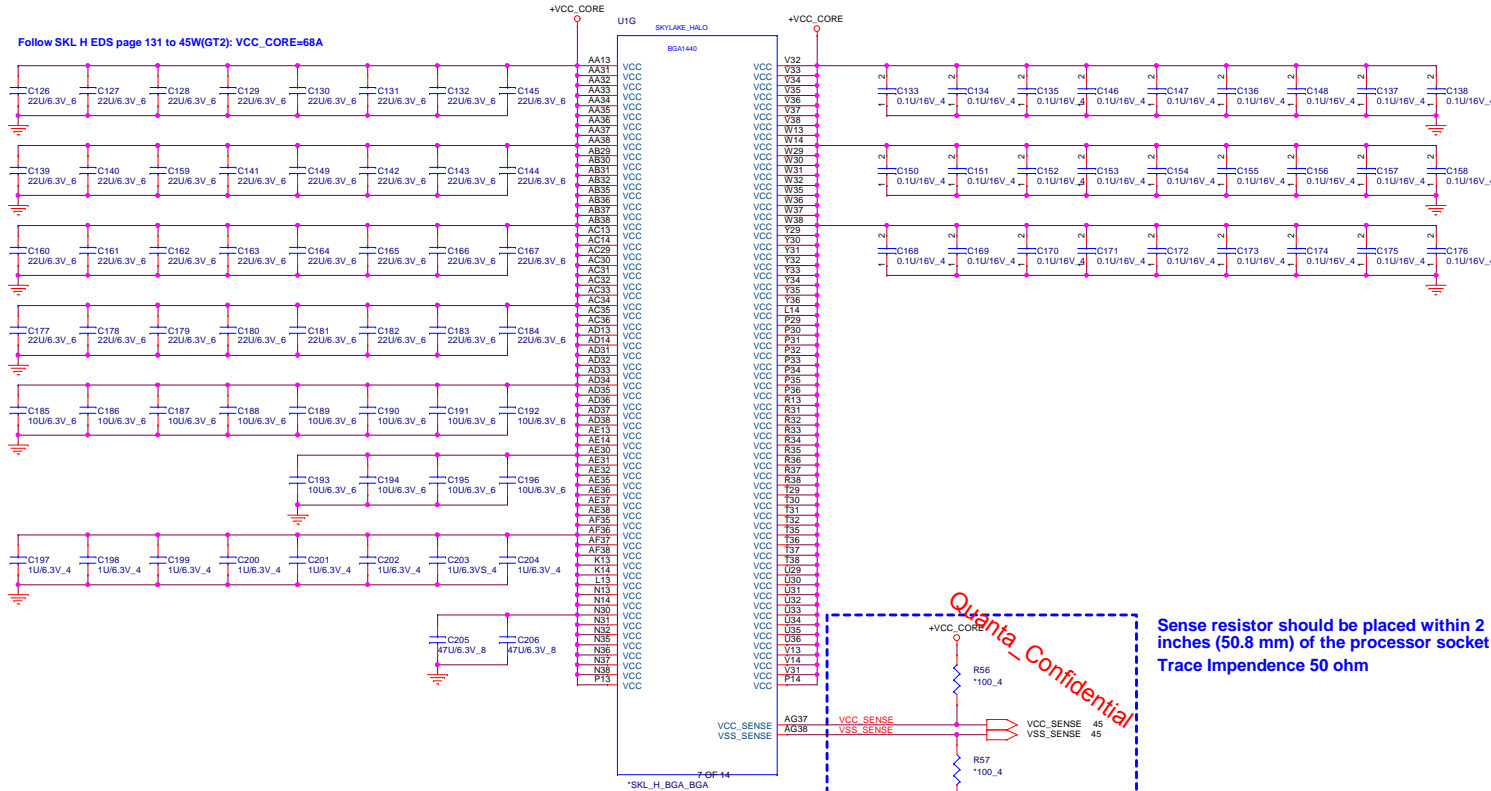
PROJECT : G38A
Quanta Computer Inc.

Size Custom	Document Number SKL 4/7 (POWER)	Rev 1A
Date: Tuesday, May 31, 2016		Sheet 5 of 56

Follow SKL H EDS page 135 45W: VDDQ=2.8A



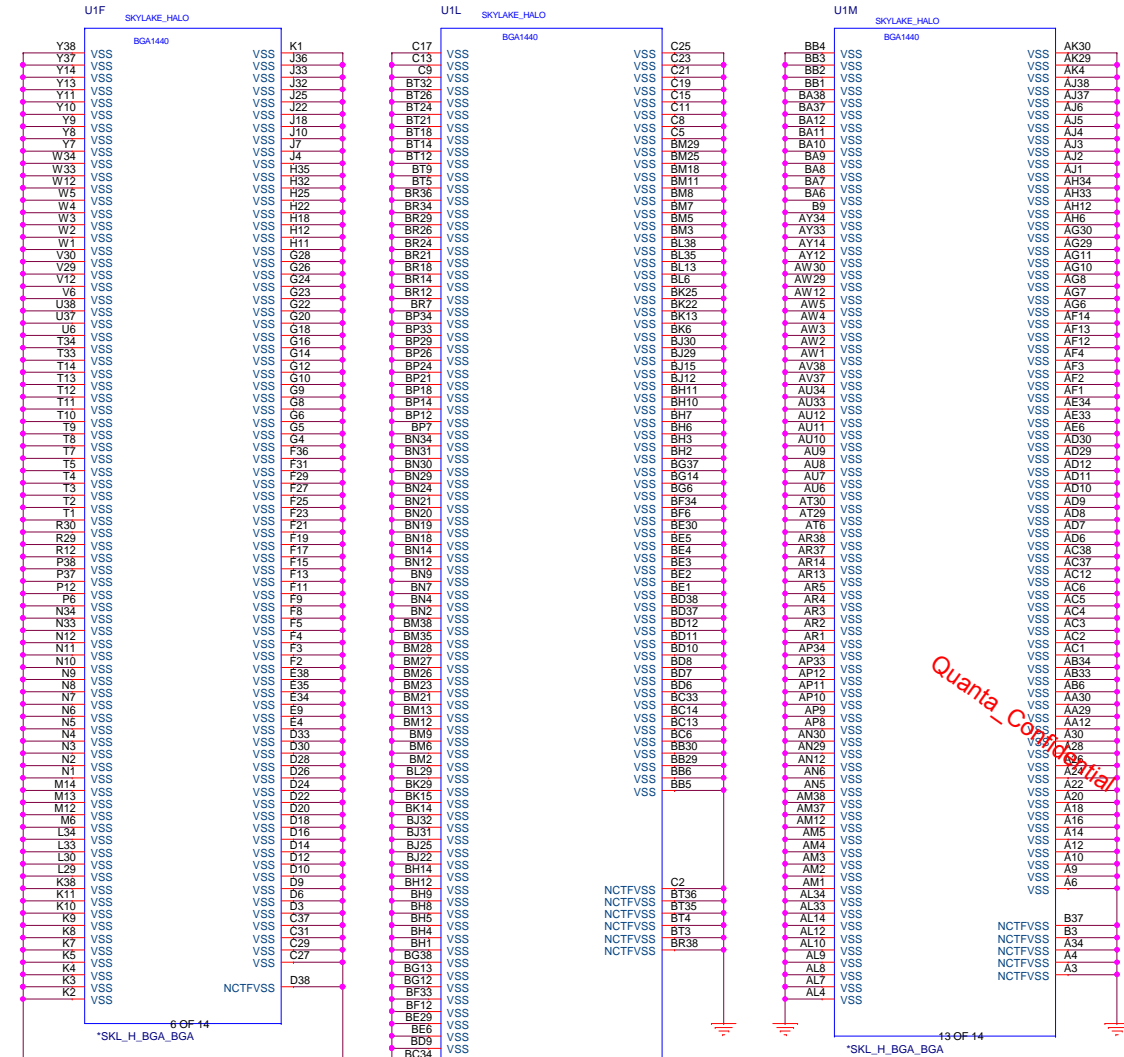
Follow SKL H EDS page 131 to 45W(GT2): VCC_CORE=68A



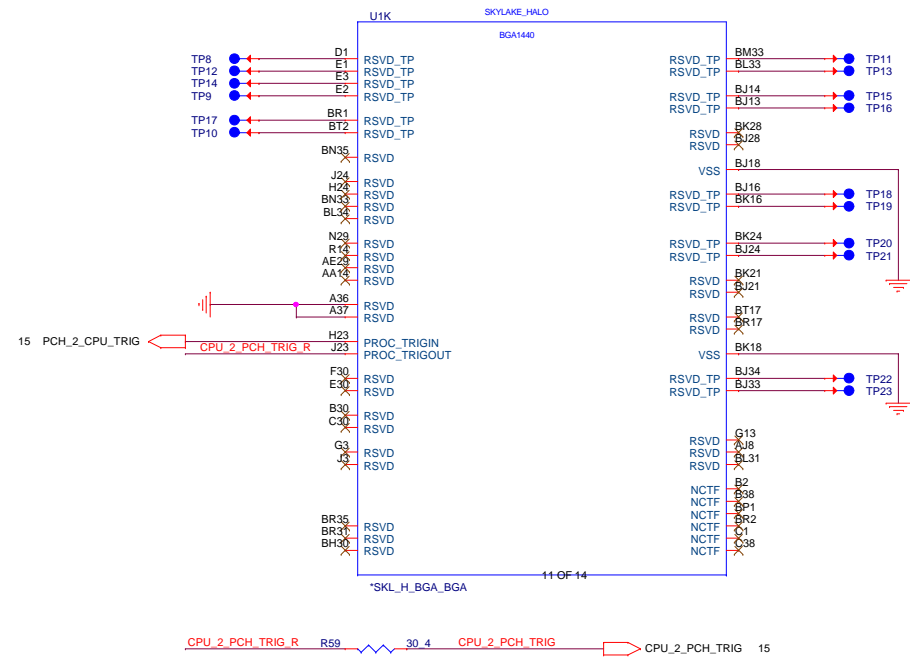
Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impedance 50 ohm

+VCC_CORE 45,46

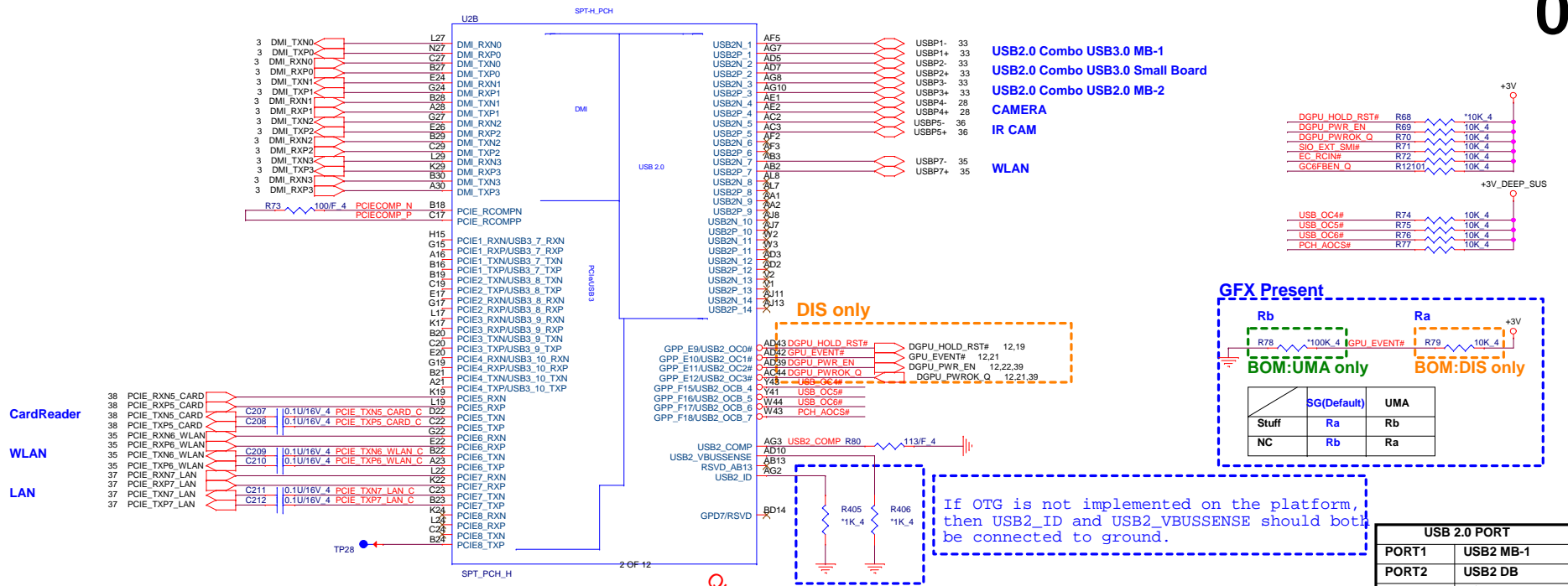
SKL-HProcessor (GND)



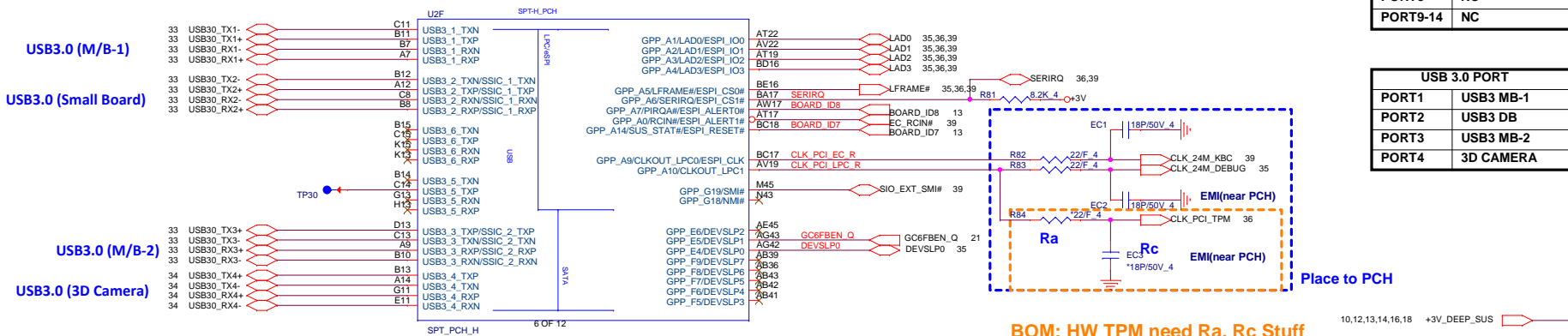
SKL-H Processor (RESERVED, CFG)

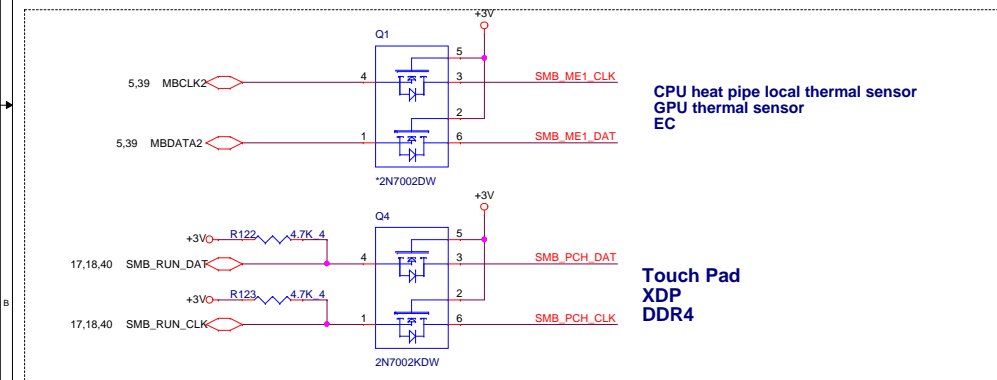
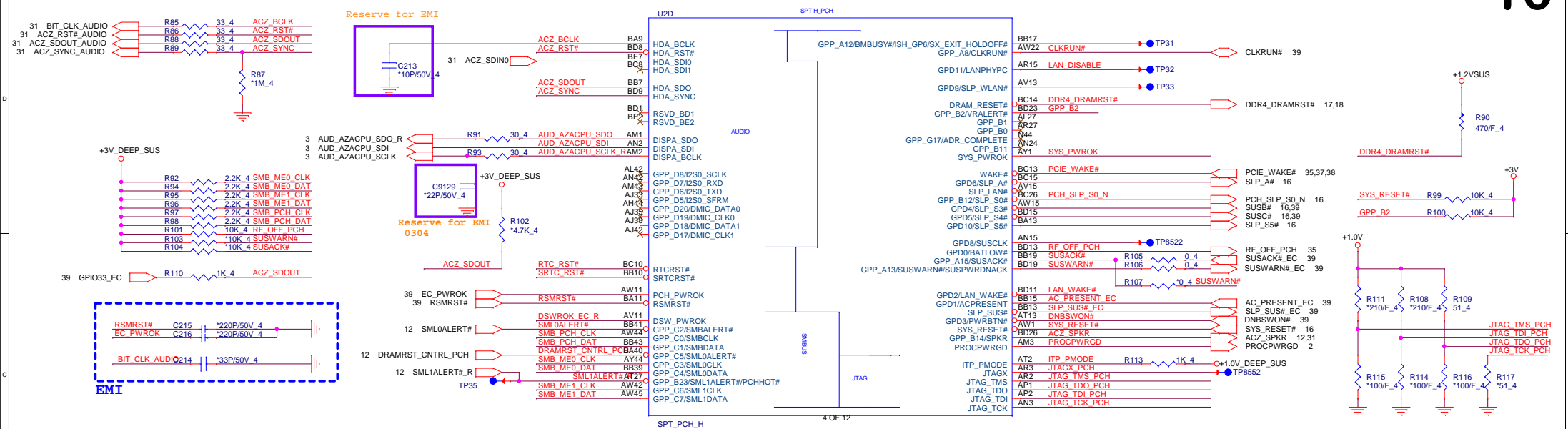


Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a Oxm board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS fro training	



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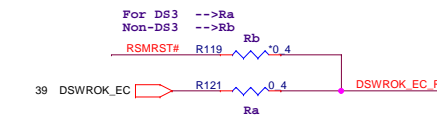




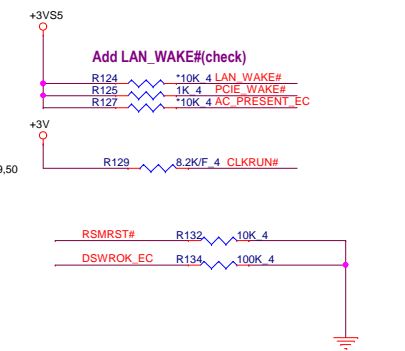
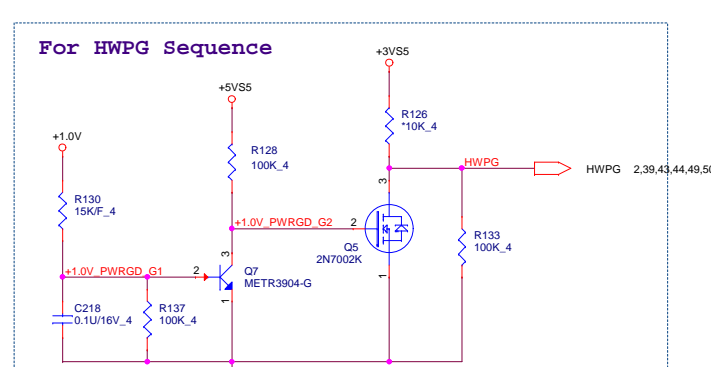
System PWR_OK(CLG)

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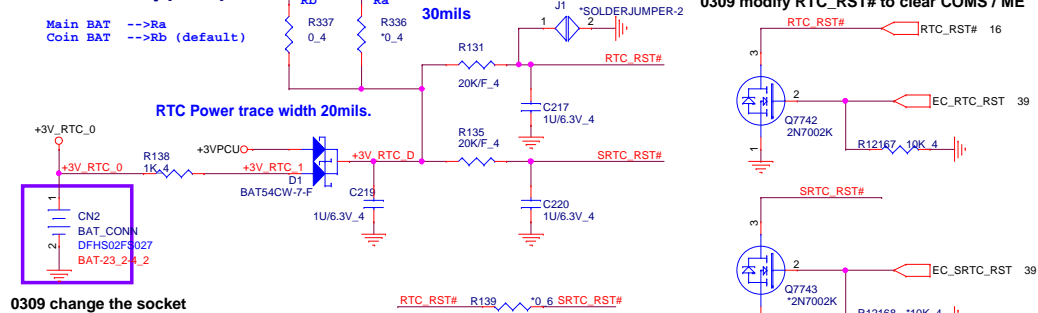
For DS3 Sequence

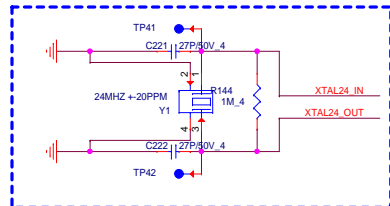


For HWP Sequence

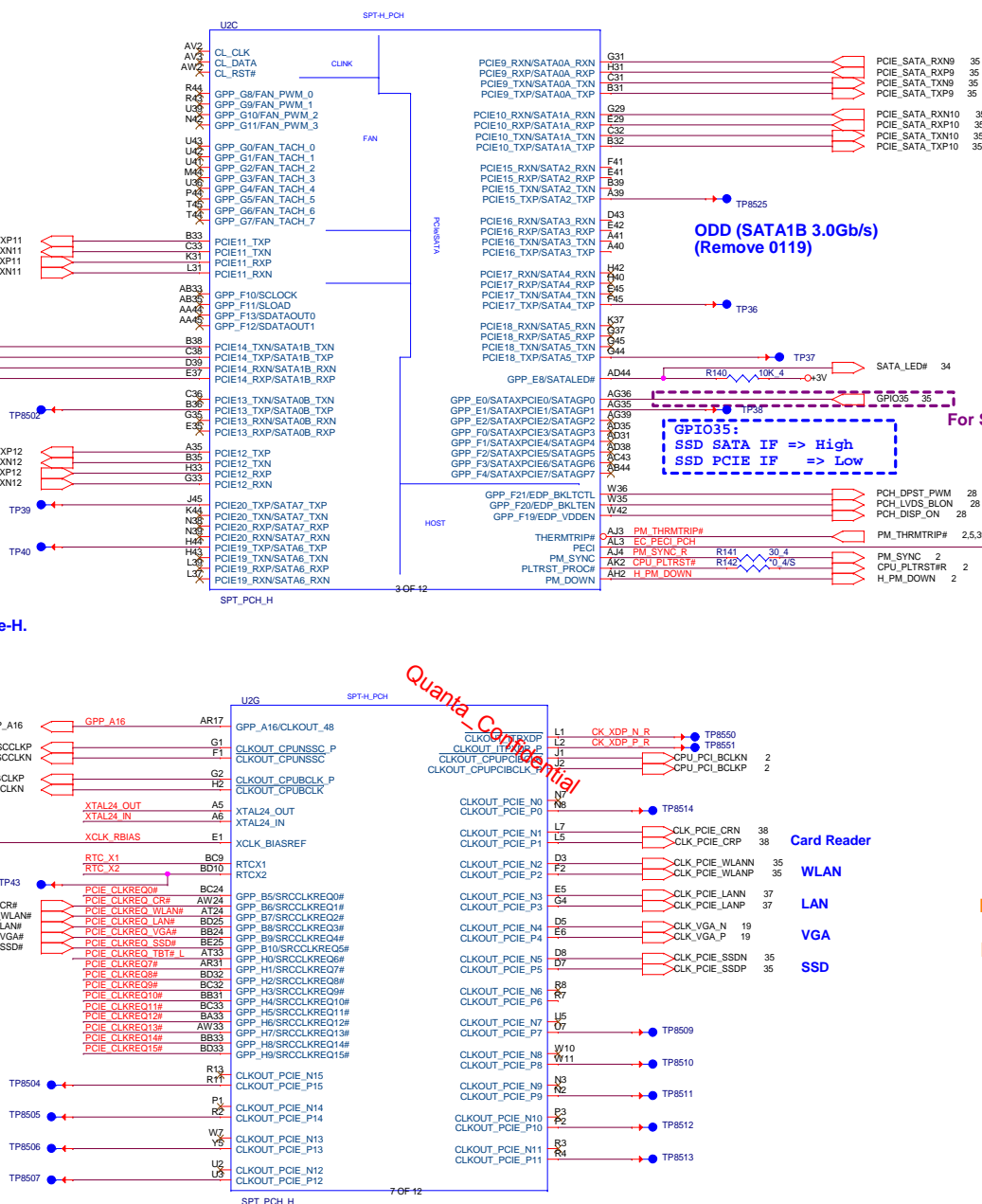
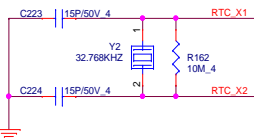


RTC Circuitry(RTC)





RTC Clock 32.768KHz

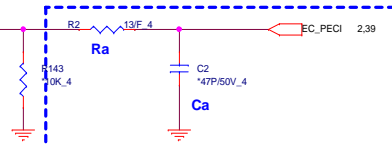


SSD PCIE x4 LANE

ODD (SATA1B 3.0Gb/s)
(Remove 0119)

For SSD Det (SATA0A)

BOM:SSD only



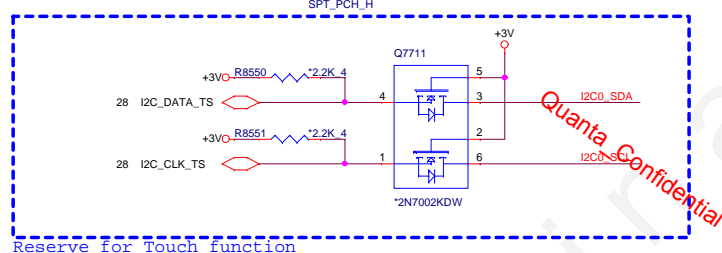
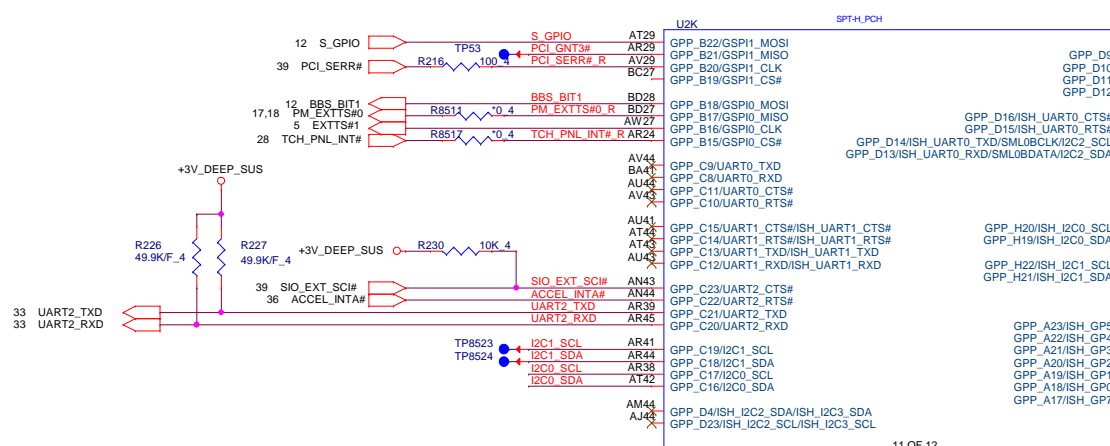
H_PECI (50ohm)
Trace Length: <0.5 inches
Ra,Ca need placement close to PCH.

Card Reader

BOM:DIS only

BOM:SSD only

PCIE_CLKREQ_WLAN#	R148	*10K_4
PCIE_CLKREQ_LAN#	R149	*10K_4
PCIE_CLKREQ_CW#	R151	*10K_4
PCIE_CLKREQ_VID#	R152	*10K_4
PCIE_CLKREQ0#	R153	*10K_4
PCIE_CLKREQ_SS0#	R154	*10K_4
PCIE_CLKREQ_TB1#_L	R155	*10K_4
PCIE_CLKREQ7#	R156	*10K_4
PCIE_CLKREQ8#	R157	*10K_4
PCIE_CLKREQ9#	R158	*10K_4
PCIE_CLKREQ10#	R159	*10K_4
PCIE_CLKREQ11#	R160	*10K_4
PCIE_CLKREQ12#	R161	*10K_4
PCIE_CLKREQ13#	R163	*10K_4
PCIE_CLKREQ14#	R164	*10K_4
	R165	*10K_4



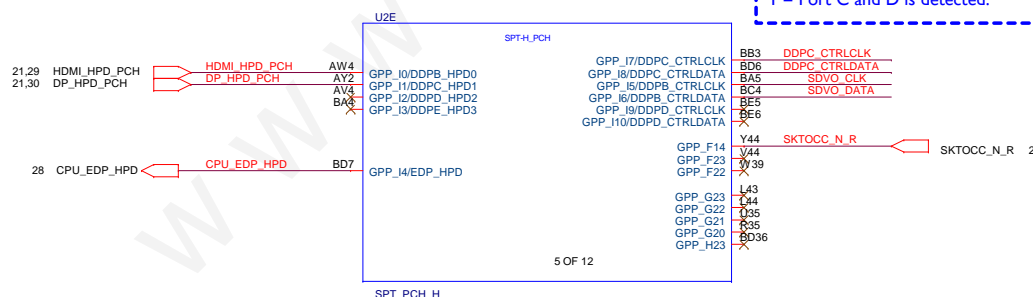
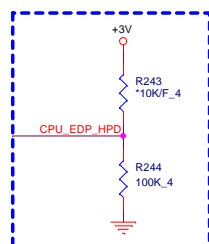
Smart AMP Setting

	Codec OUTPUT	AMP OUTPUT
GPIO	GPP_D11 SPK_ID	GPP_D15 SPKAMP_ID
Definition	Hi: SABLE Low: VECO	Hi: SABLE Low: VECO

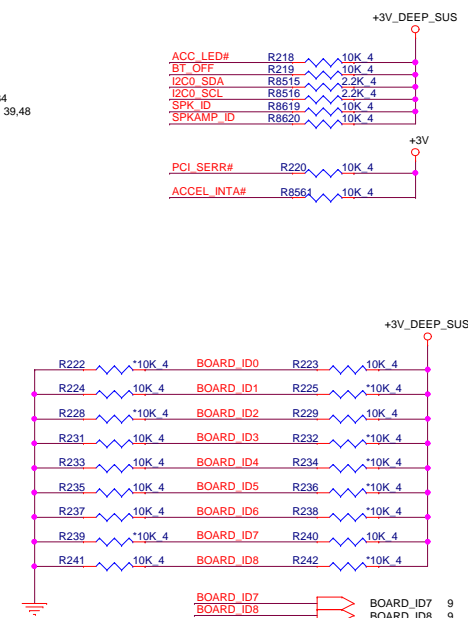
Board ID

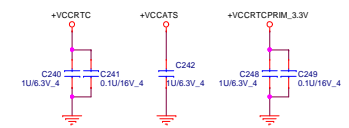
Model	BOARD_ID[8:7] ID8;ID7	BOARD_ID[6:5] ID6;ID5	Board ID [4:3]	BOARD_ID[2:1] ID2;ID1	BOARD_ID0 ID0
Definition	01 SKL H	00 Reserved	ID4 Reserve	ID3 0 NVidia 1 AMD	00 15" P SKL H 01 17" P SKL H 10 17" SP SKL H 11 Reserved

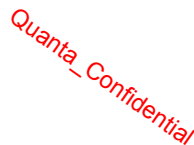
Reserve EDP_HPDP opposites circuit!



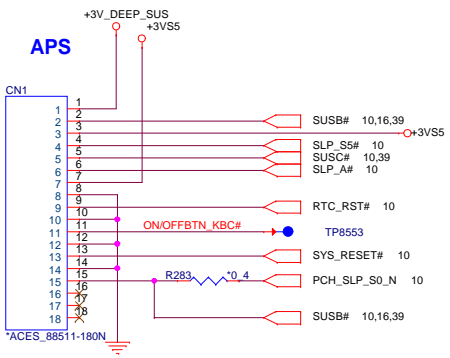
This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.



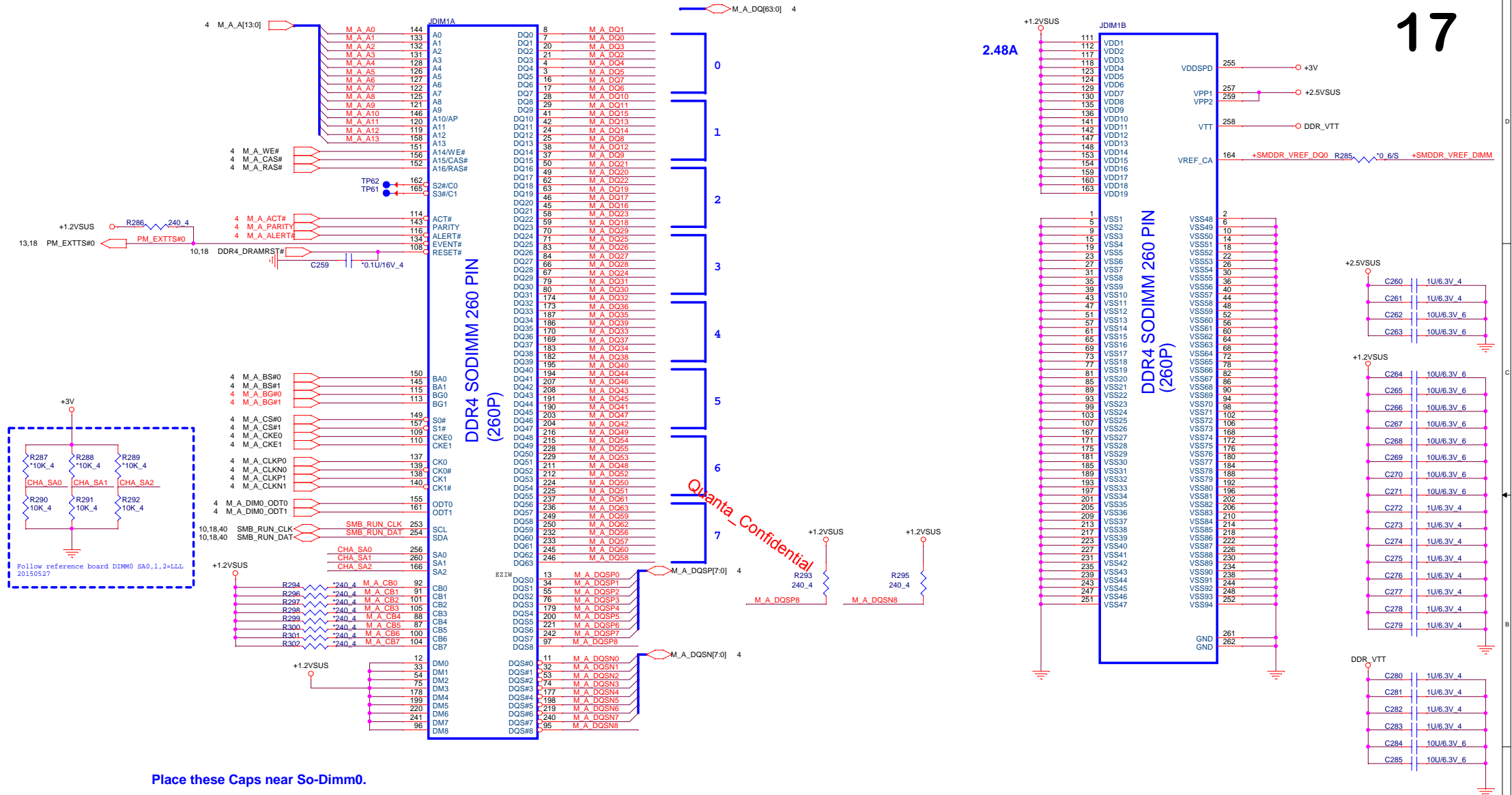




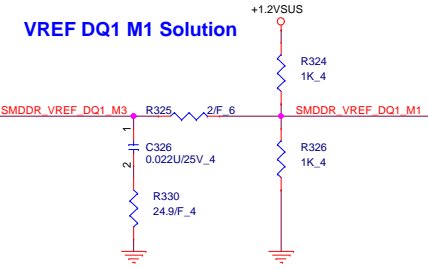
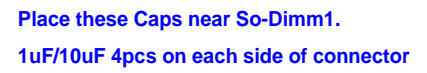
Quanta_Confidential

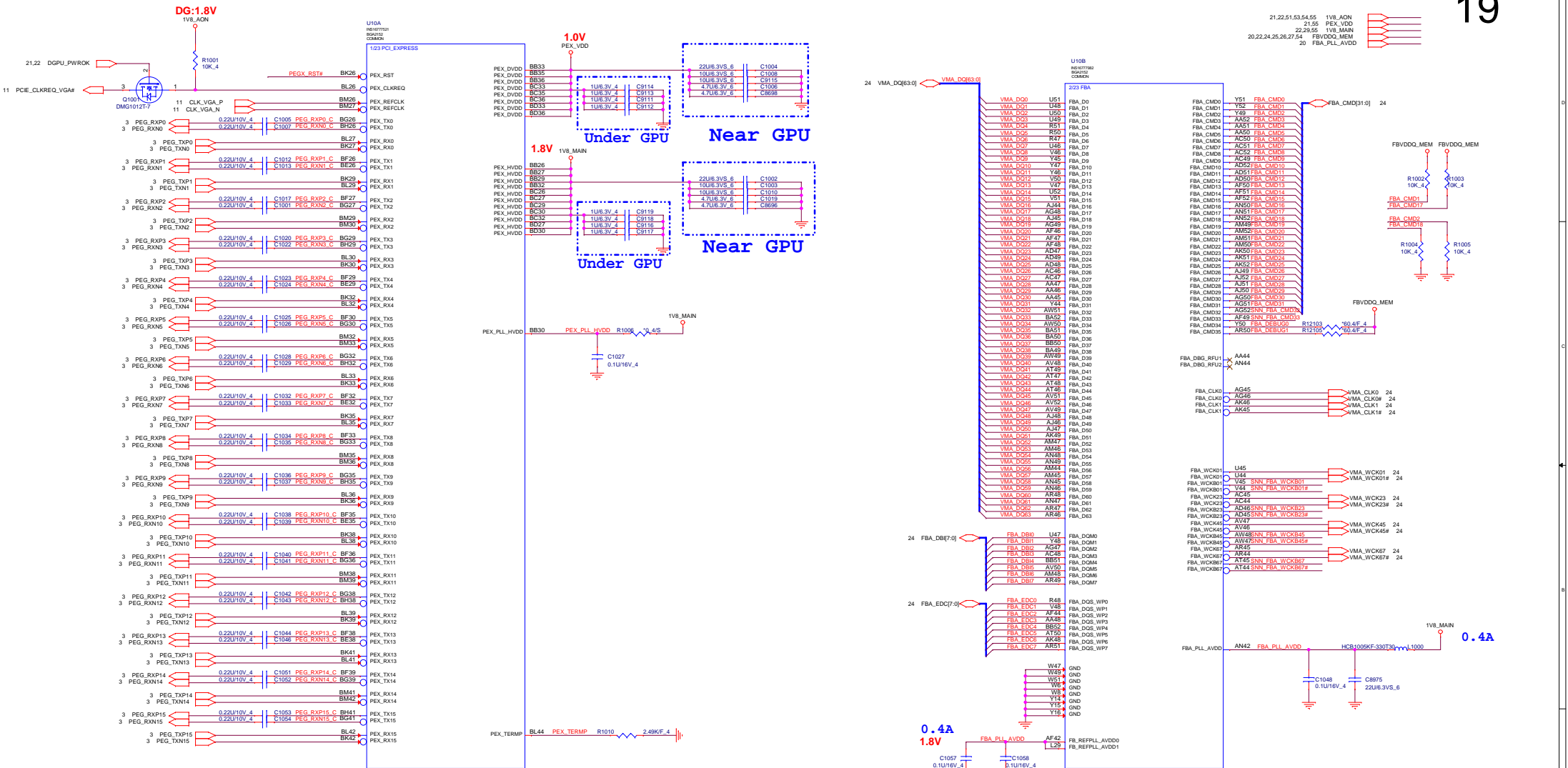


9,10,12,13,14,18 +3V_DEEP_SUS

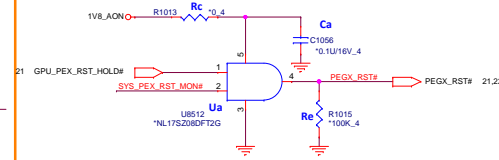
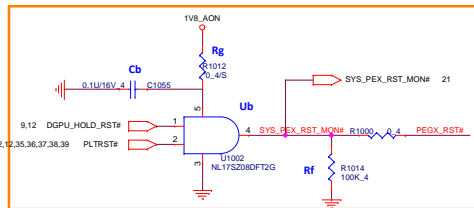


+2.5VSUS 18,44
 DDR_VTT 18,44
 +1.2VSUS 2,6,10,18,44,50,55
 +3V 5,9,10,11,12,13,14,18,21,22,28,29,30,31,32,33,34,35,36,37,38,39,40,45,48,54,55

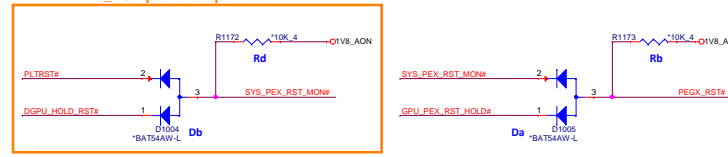


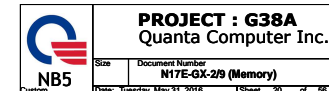


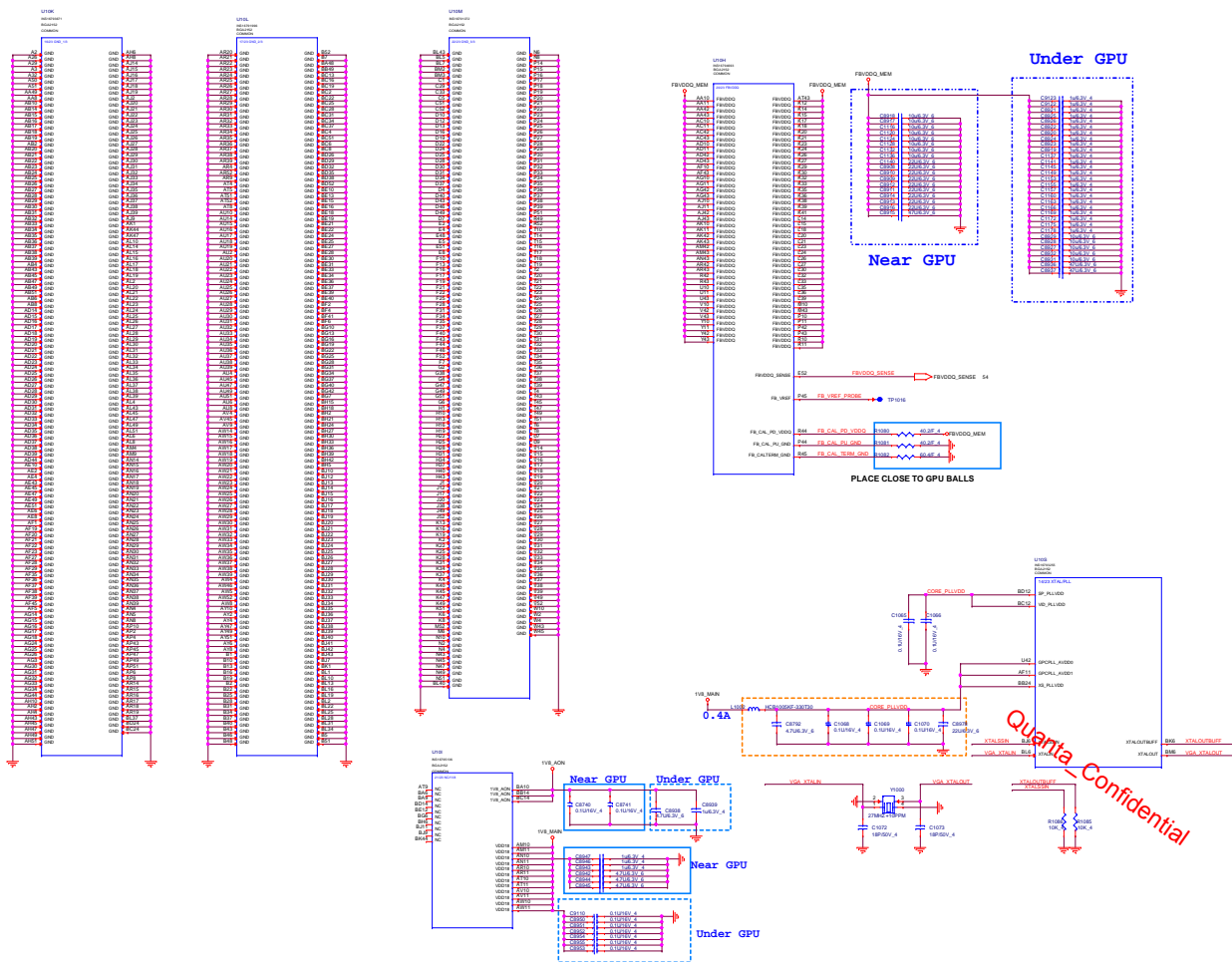
N17_GPU RST#

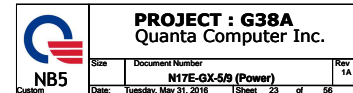


N17_RST power sequence









Channel 0
<0~31>

MF=1 mirrored

MF=0 Non-mirrored

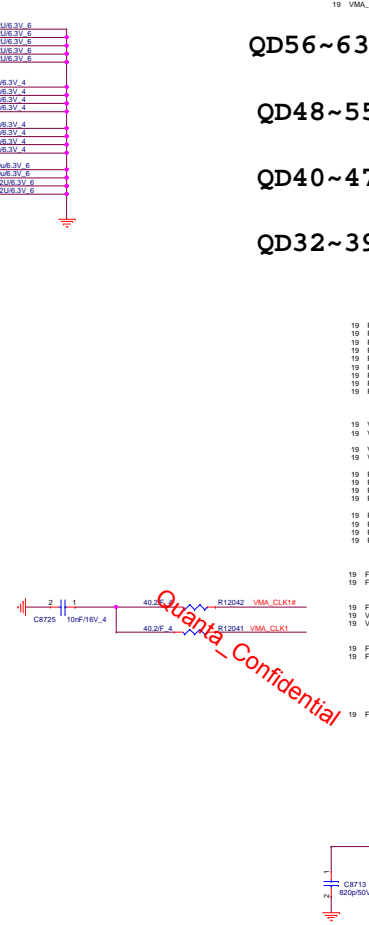
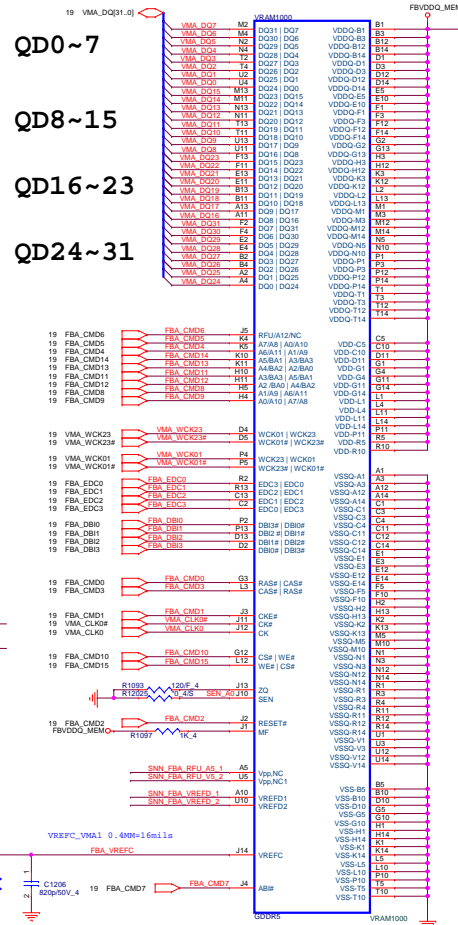
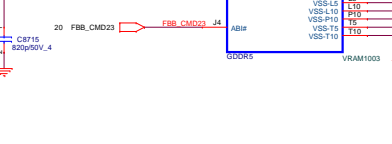
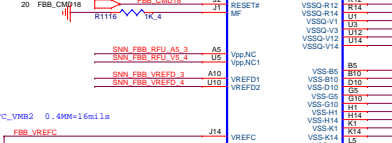
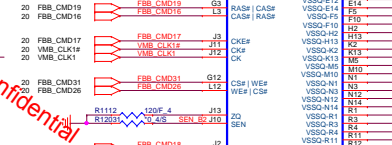
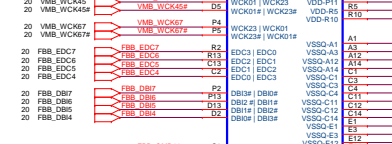
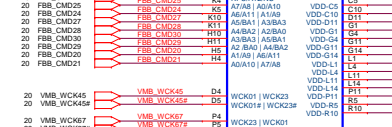
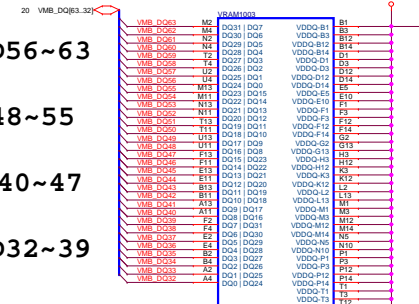


Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CM00	CAS*	CM016	CAS*
CM01	CKE	CM017	CKE
CM02	RST*	CM018	RST*
CM03	RA*	CM019	RA*
CM04	A1_A9	CM020	A1_A9
CM05	A0_A10	CM021	A0_A10
CM06	A4_RFU	CM022	A12_RFU
CM07	AB*	CM023	AB*
CM08	A6_A11	CM024	A6_A11
CM09	A7_A8	CM025	A7_A8
CM10	WE*	CM026	WE*
CM11	A5_BA1	CM027	A5_BA1
CM12	A4_BA2	CM028	A4_BA2
CM13	A2_BA0	CM029	A2_BA0
CM14	A3_BA3	CM030	A3_BA3
CM15	CS*	CM031	CS*

Notes:
1. Gpu debug pins; not connected to DRAM. See section 7.1.13.

Non-mirr



Notes:

1. GPU debug pins; not connected to DRAM. See section 7.1.13.

Channel 0
<0-31>

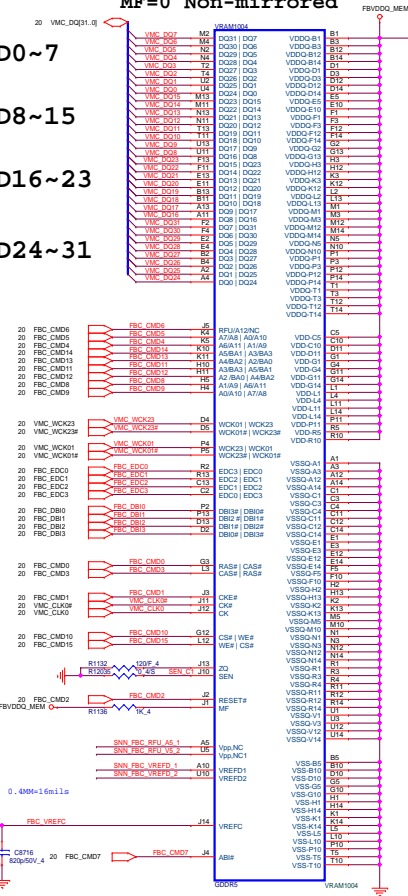
MF=0 Non-mirrored

QD0~7

QD8~15

QD16~23

QD24~31



Channel 1
<0-31>

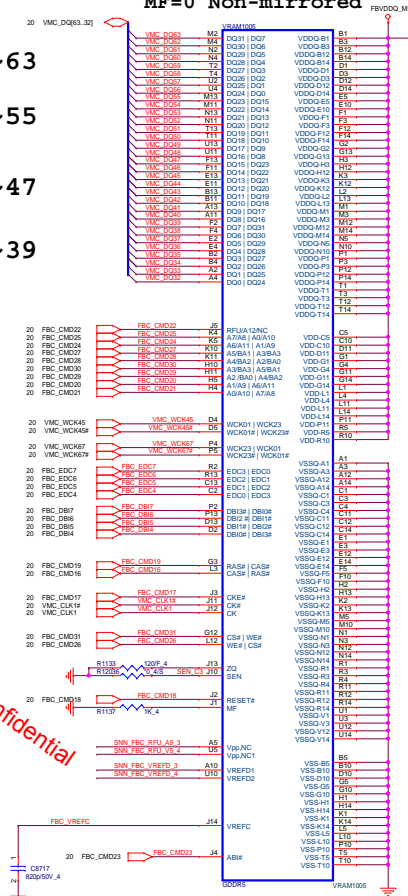
MF=0 Non-mirrored

QD56~63

QD48~55

QD40~47

QD32~39



19.20.22.24.26.27.54

FBVDDQ_MEM

Table 7-5. GDDR5 Mode F Mapping

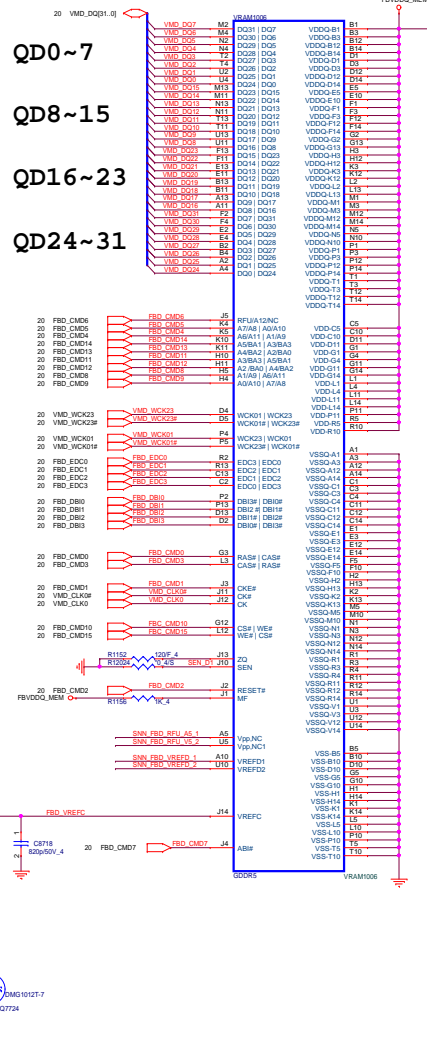
GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RA5*	CMD19	RA5*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	AB*	CMD23	AB*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	C5*	CMD31	C5*
GB3-256 Channel 0 B 1			
CMD32	Hot used		
CMD33	Hot used		
CMD34	DEBUG*		
CMD35	DEBUG*		

Notes:

1. GPU debug pins; not connected to DRAM. See section 7.1.13.

Channel 0
<0-31>

MF=1 mirrored

Channel 1
<0-31>

MF=0 Non-mirrored

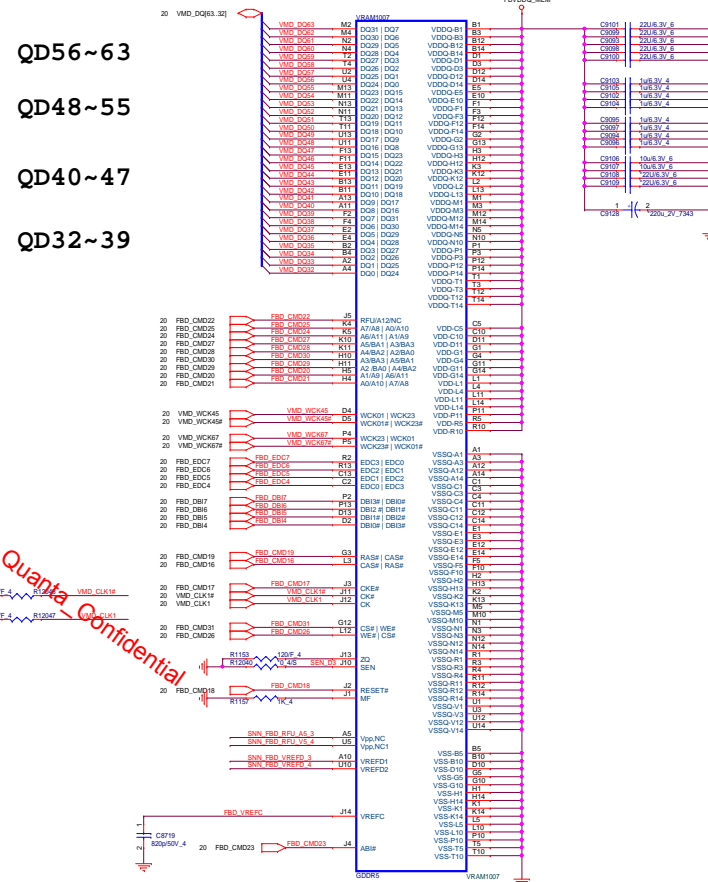
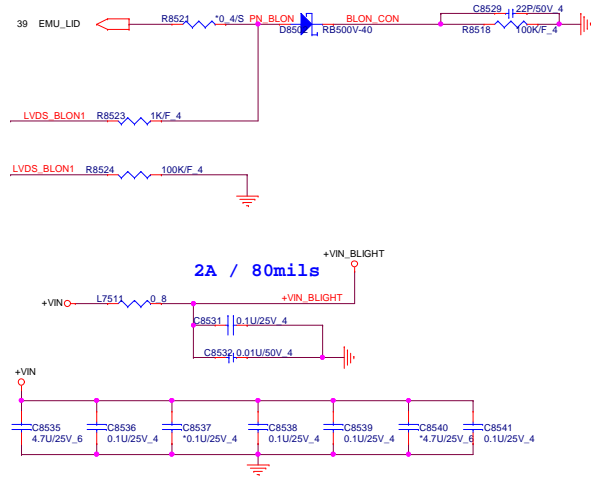


Table 7-5. GDDR5 Mode F Mapping

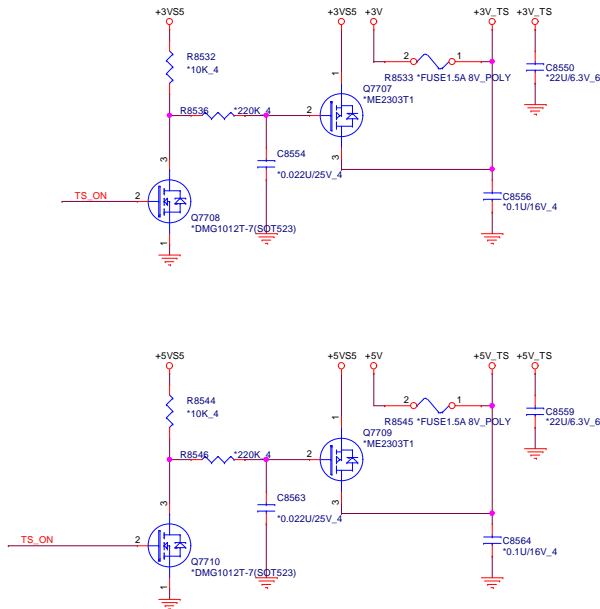
GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CM00	CAS*	CM016	CAS*
CM01	CKE	CM017	CKE
CM02	RST*	CM018	RST*
CM03	RAS*	CM019	RAS*
CM04	A1_A9	CM020	A1_A9
CM05	A0_A10	CM021	A0_A10
CM06	A12_RFU	CM022	A12_RFU
CM07	AB1*	CM023	AB1*
CM08	A6_A11	CM024	A6_A11
CM09	A7_A8	CM025	A7_A8
CM10	WE*	CM026	WE*
CM011	A5_BA1	CM027	A5_BA1
CM012	A4_BA2	CM028	A4_BA2
CM013	A2_BA0	CM029	A2_BA0
CM014	A3_BA3	CM030	A3_BA3
CM015	CS*	CM031	CS*
GB3-256	Channel 0 B 1		
CM032	Hot used		
CM033	Hot used		
CM034	DEBUG*		
CM035	DEBUG*		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

LID Switch



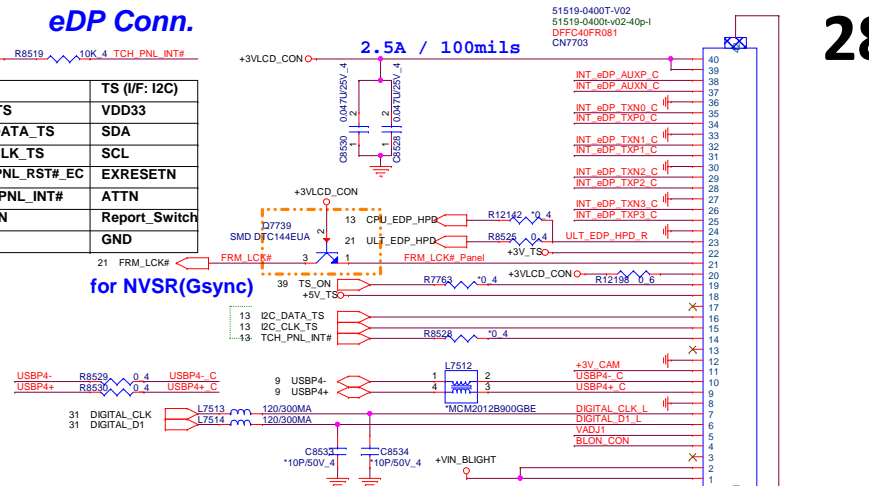
Reserve for Touch screen



eDP Conn.

MB	TS (I/F: I2C)
+3V_TS	VDD33
I2C_DATA_TS	SDA
I2C_CLK_TS	SCL
TCH_PNL_RST#_EC	EXRESETN
TCH_PNL_INT#	ATTN
TS_ON	Report_Switch
GND	GND

for NVSR(Gsync)



C9132/C8542(Back to Back)
C9131/C8543(Back to Back)

CPU/GPU EDP
co-layer

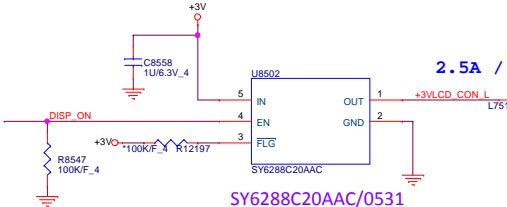
C9134/C8544(Back to Back)
C9133/C8547(Back to Back)

Quanta Confidential

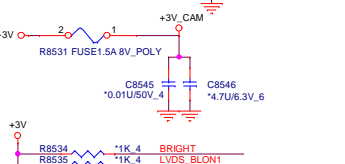
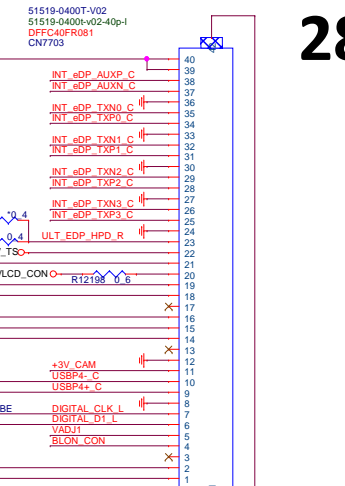
CPU/GPU EDP
co-layer

C9136/C8553(Back to Back)
C9135/C8545(Back to Back)

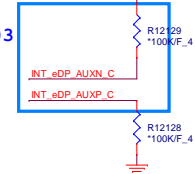
CPU/GPU EDP
co-layer



SY6288C20AAC/0531

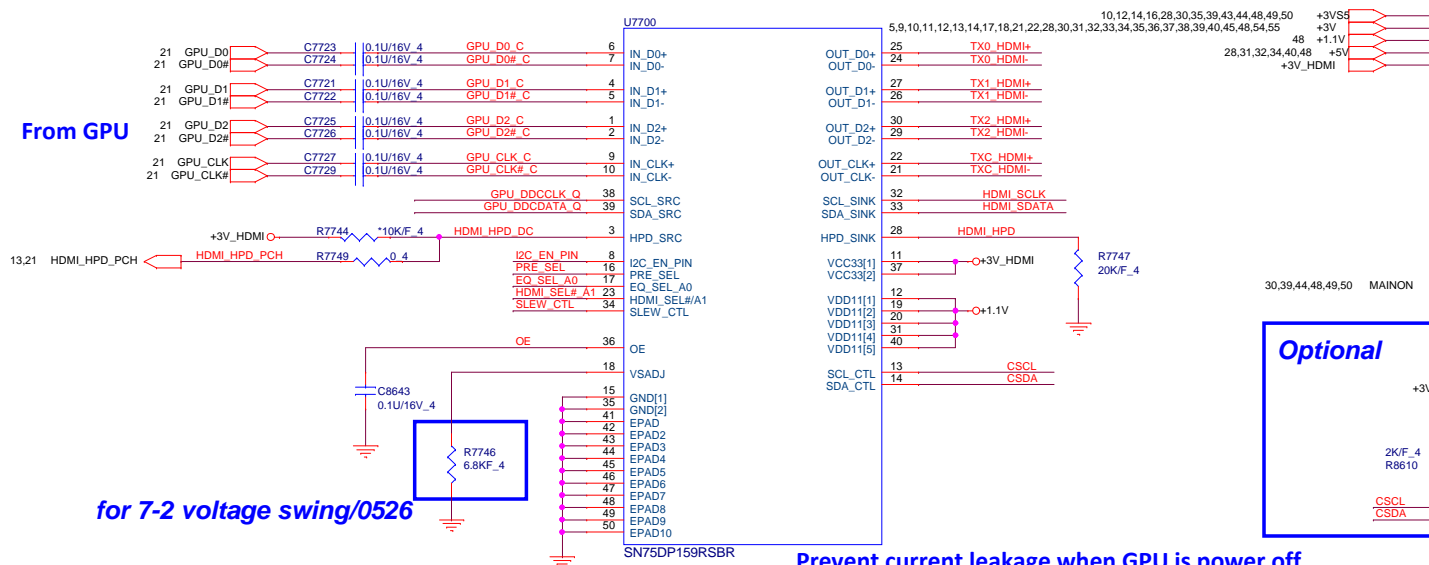


follow NV
suggest_0303



5,9,10,11,12,13,14,17,18,21,22,29,30,31,32,33,34,35,36,37,38,39,40,45,48,54,55
5,10,21,33,35,39,40,42,43,51 +3VPCU
29,31,32,34,40,48 +5V
40,41,42,43,44,45,46,47,48,49,50,51,54 +VIN

From GPU



Prevent current leakage when GPU is power off
add R12317/R1231 is for HDMI verify

SN75DP159RSBR strap

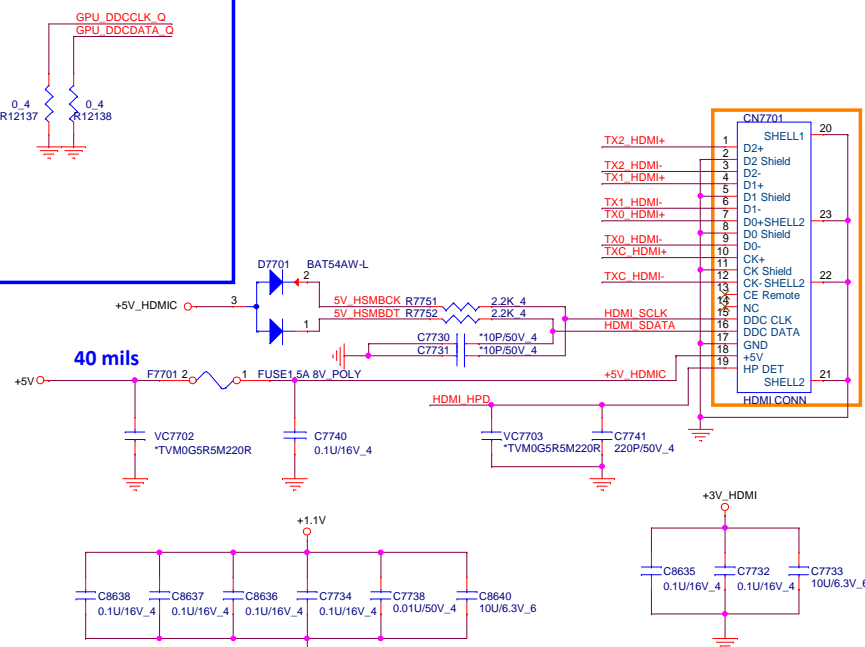
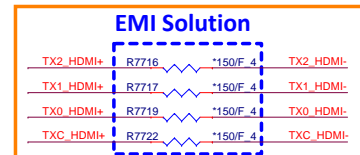
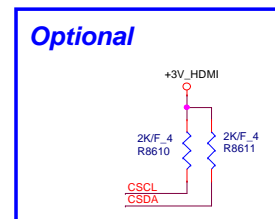
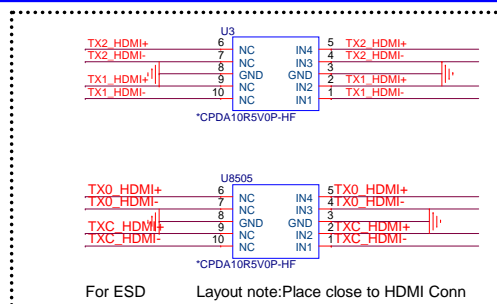
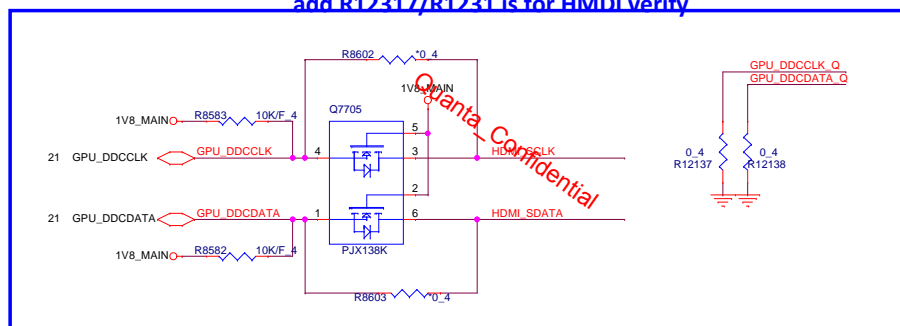
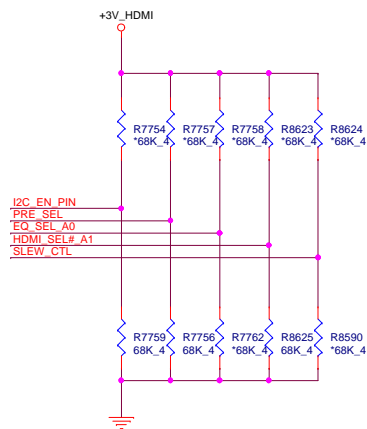
I2C_EN/PIN = High: puts device into I2C control mode
I2C_EN/PIN = Low: puts device into pin strap mode

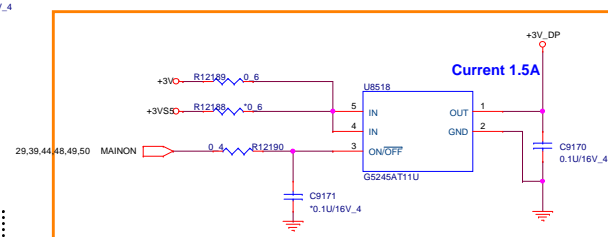
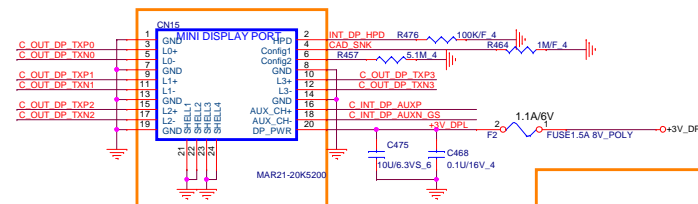
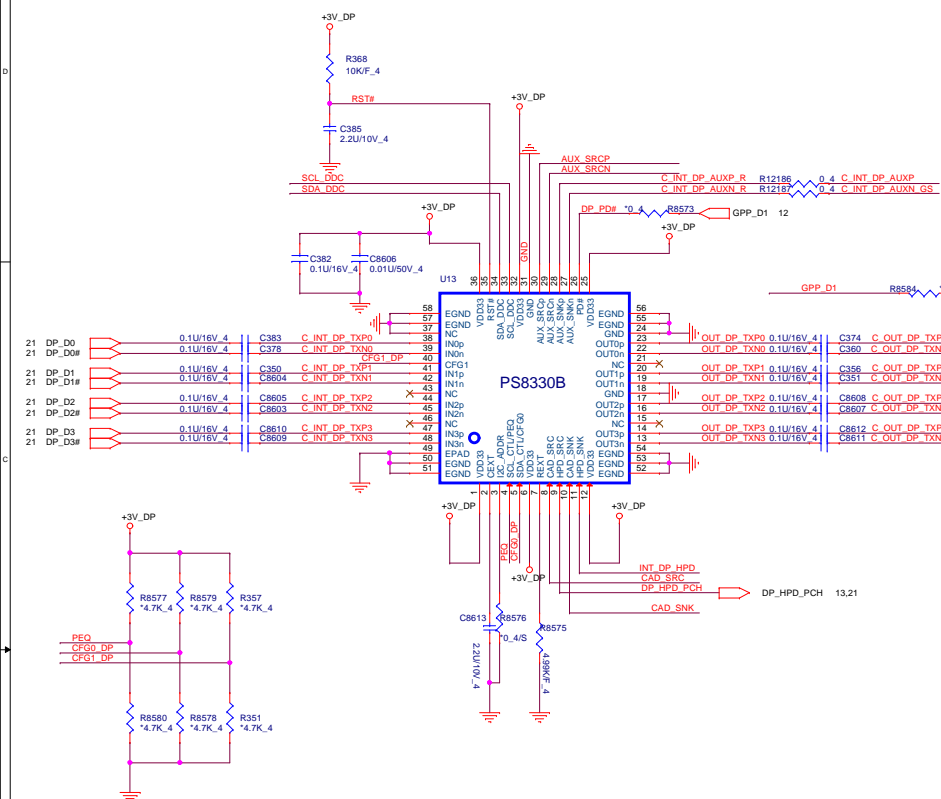
De-emphasis pin strap when I2C_EN/PIN = Low.
PRE_SEL = L: - 2 dB de-emphasis
PRE_SEL = No Connect: 0 dB
PRE_SEL = H: Reserved

Input Receive Equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L: Fixed EQ at 7.5 dB
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 14 dB

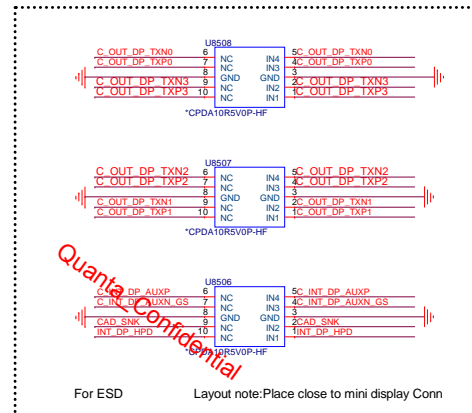
HDMI_SEL when I2C_EN/PIN = Low
HDMI_SEL = High: Device configured for DVI
HDMI_SEL = Low: Device configured for HDMI

Slew rate control when I2C_EN/PIN = Low.
SLEW_CTL = H, fastest data rate
SLEW_CTL = L, 5 ps slow
SLEW_CTL = No Connect, 10 ps slow



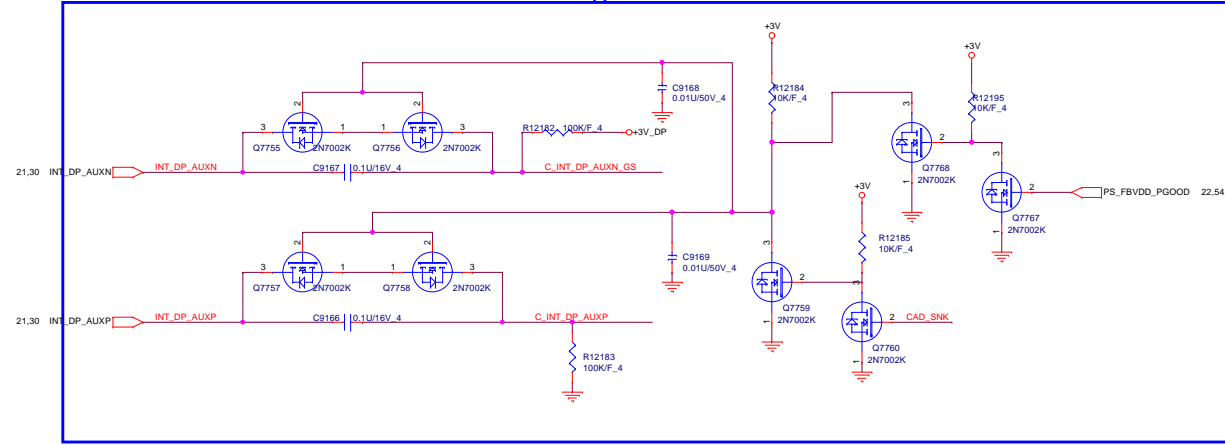
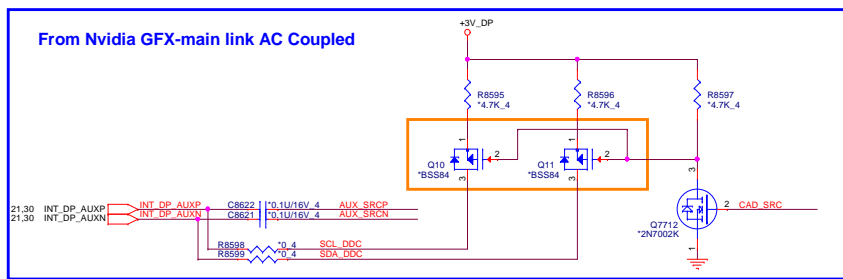


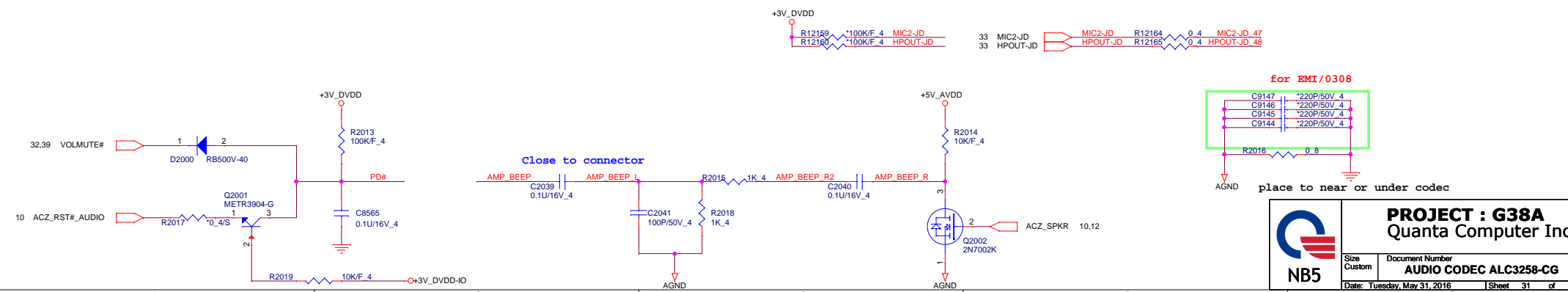
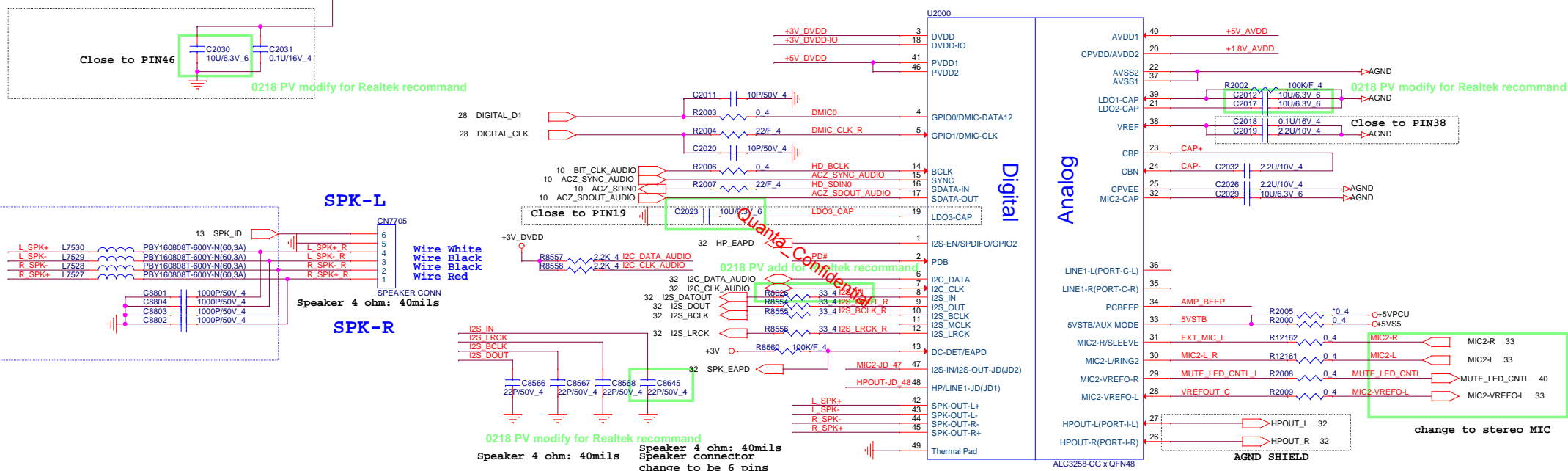
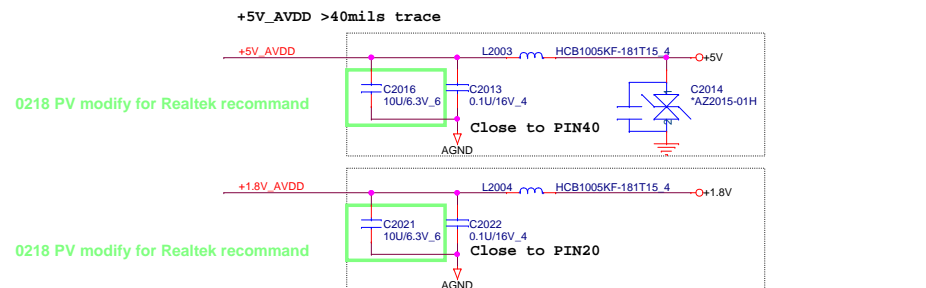
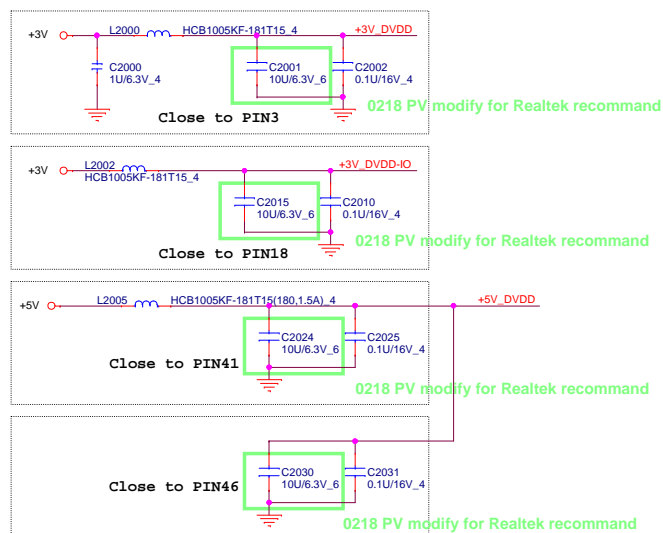
Modify GMT/0531



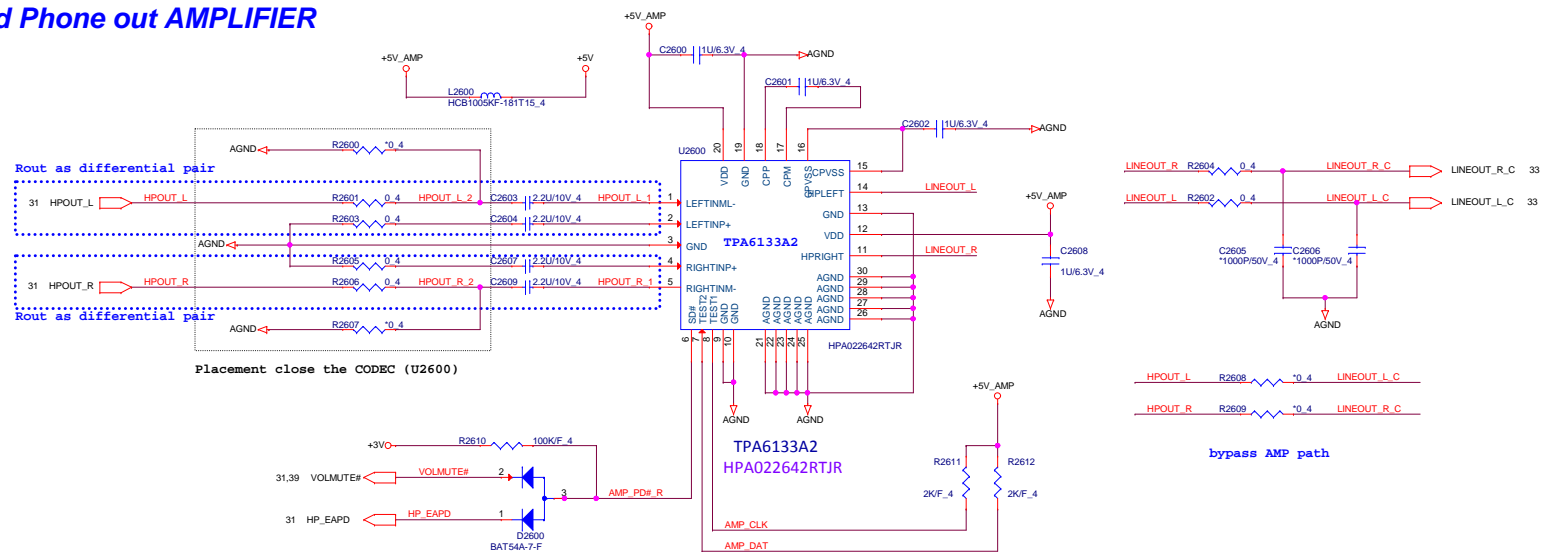
For ESD Layout note:Place close to mini display Conn

support dual mode /0525

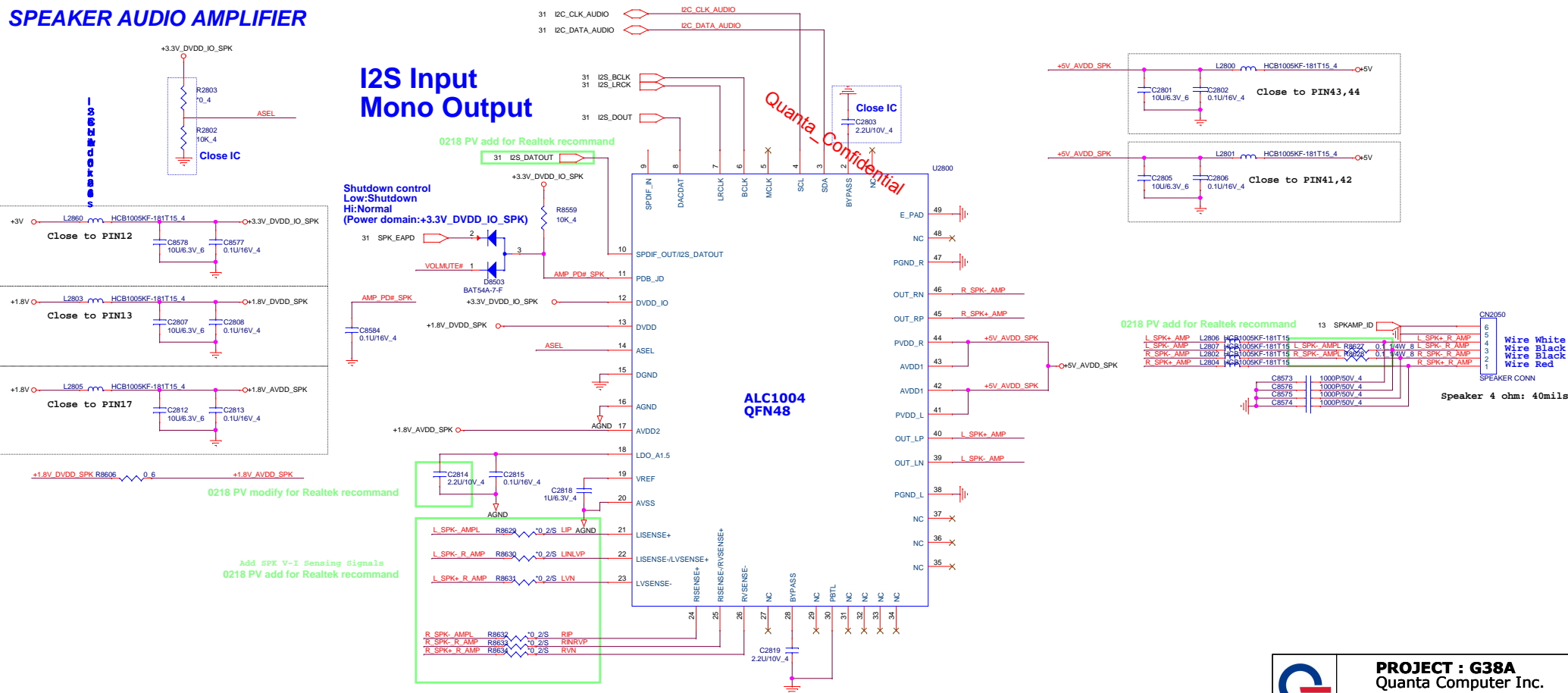


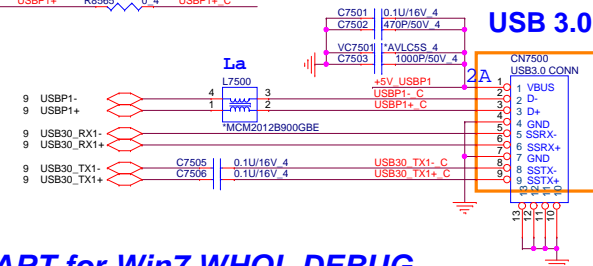
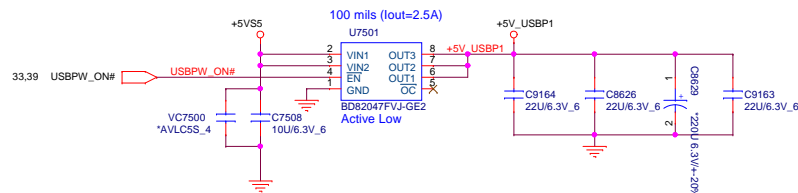


Head Phone out AMPLIFIER

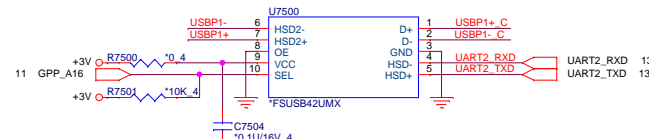


SPEAKER AUDIO AMPLIFIER

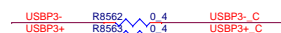




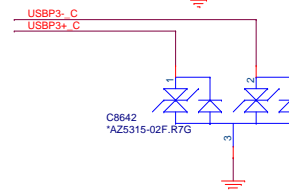
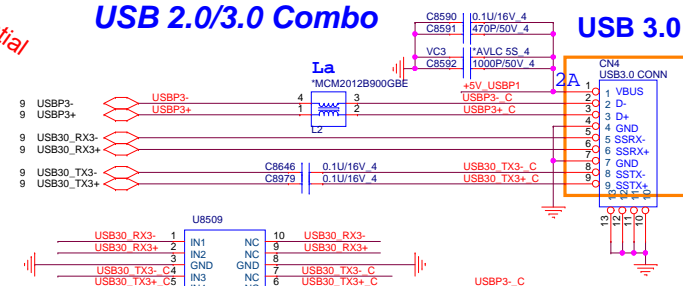
UART for Win7 WHQL DEBUG



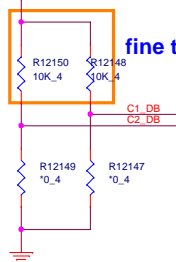
Place Back to Back La



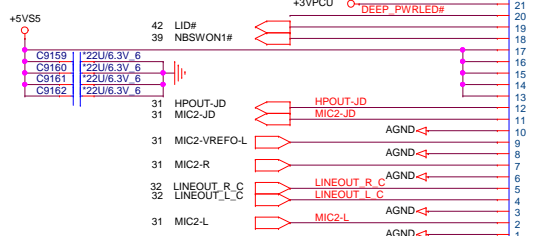
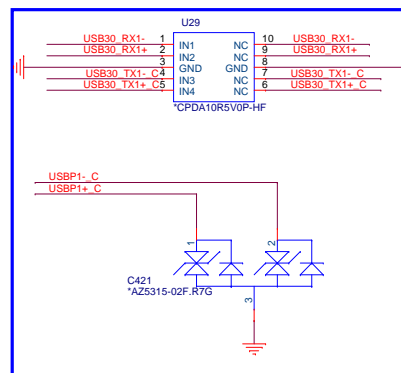
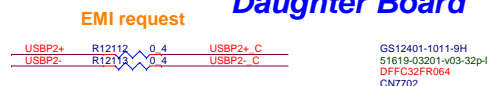
USB 2.0/3.0 Combo



fine tune 後eye pass

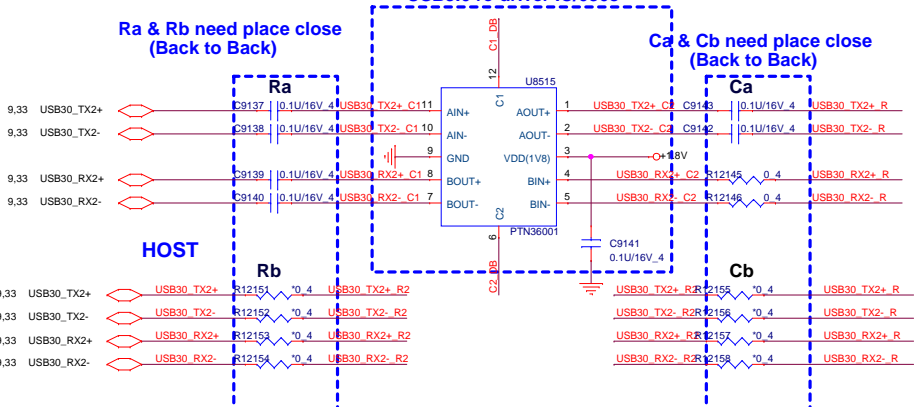


Daughter Board

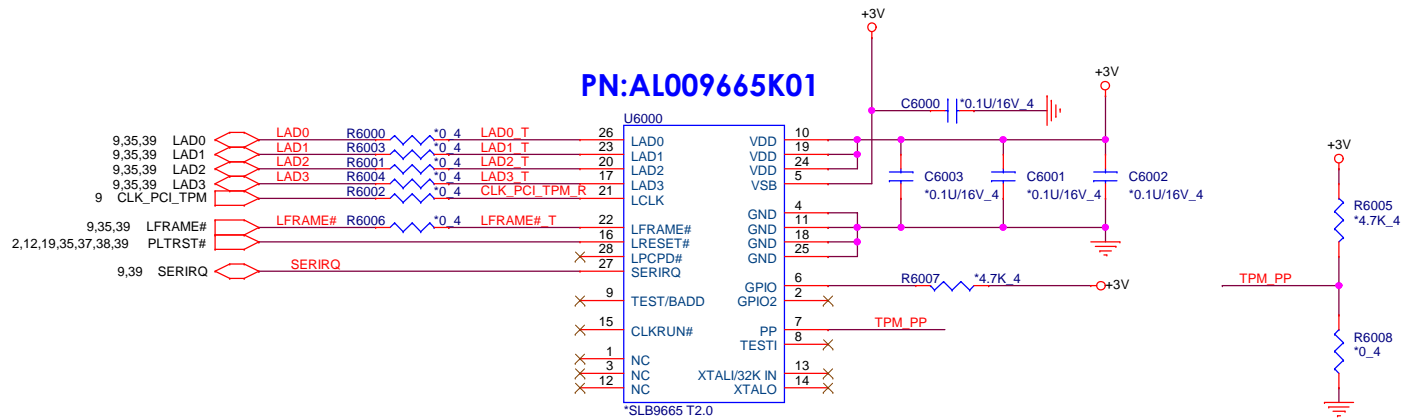


change to stereo MIC/0308

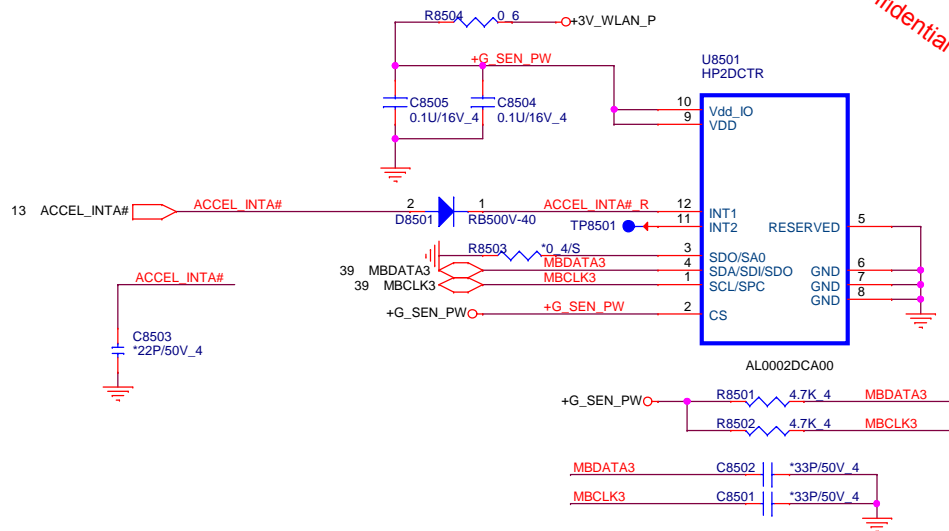
USB3.0 re-driver IC/0308



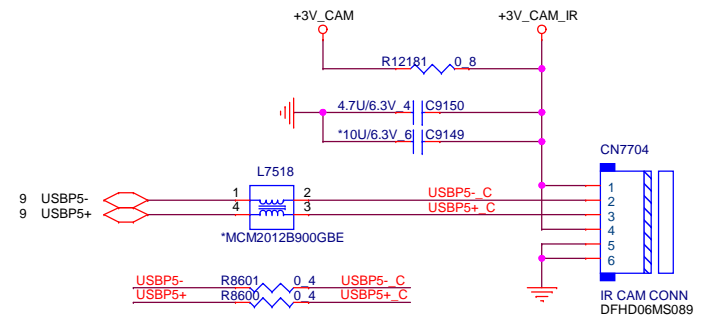
TPM (2.0)



Accelerometer Sensor



IR CAM



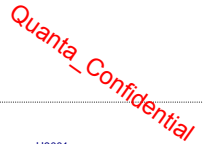
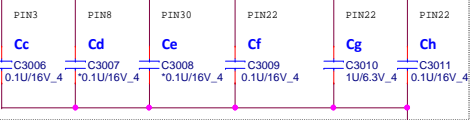
PROJECT : G38A
Quanta Computer Inc.

Size	Document Number TPM/G-Sensor/IR CAM	Rev 1A
Date: Tuesday, May 31, 2016		Sheet 36 of 56

Stuff La, Ca ,Cb

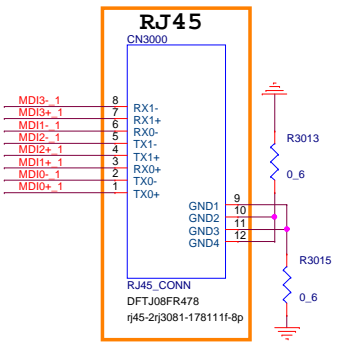
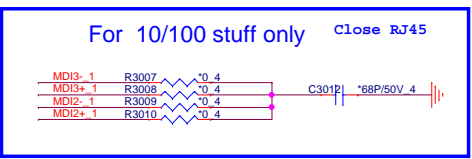
Power trace Layout 寬度> 60mil

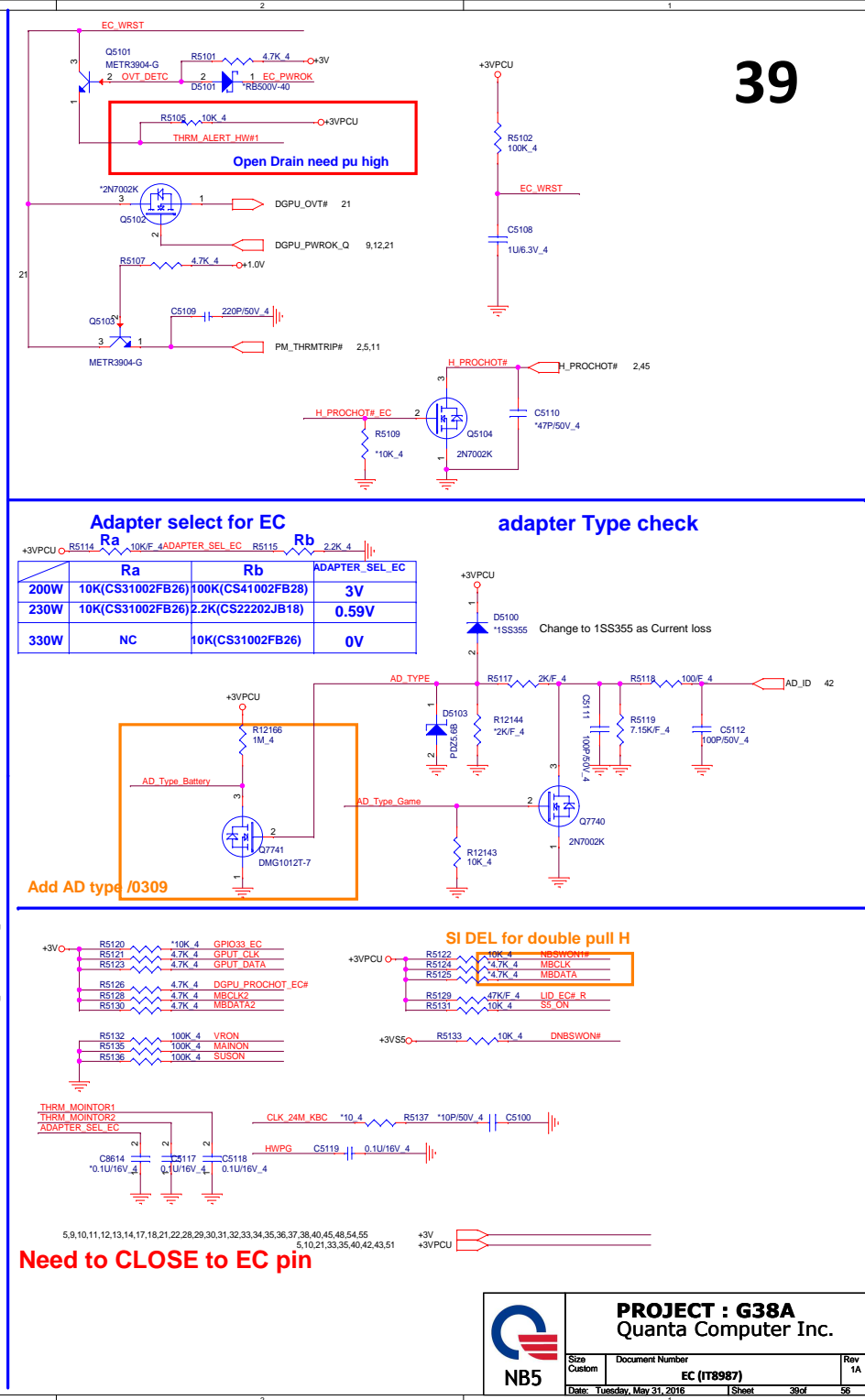
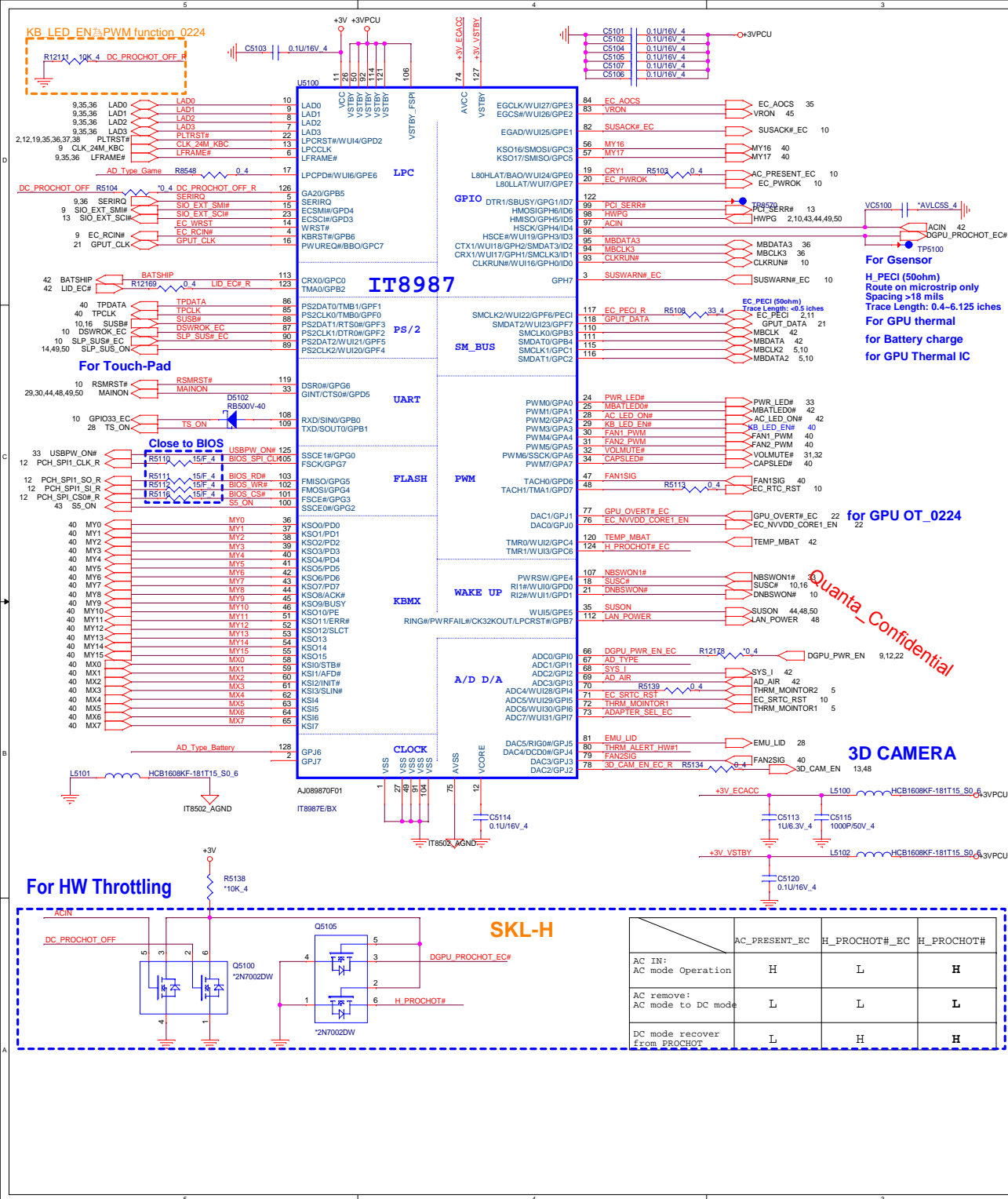
>60mil >60mil



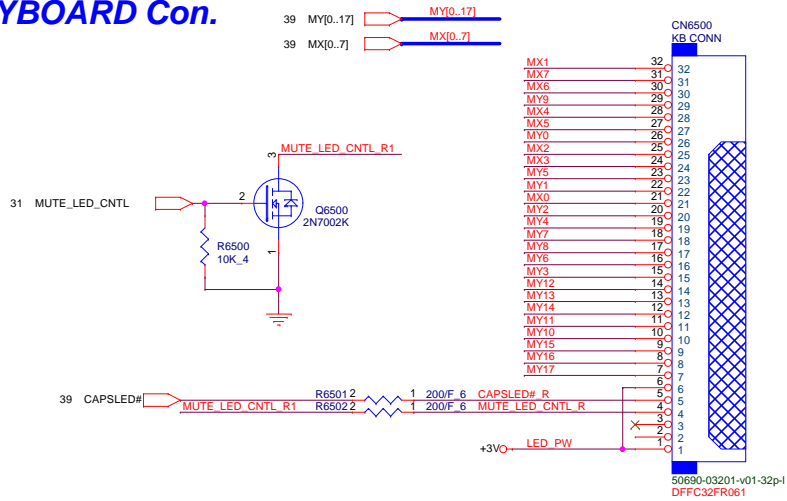
For SWR mode support RTL8111HSH/RTL8107ESH
Stuff Co, Cp

The diagram shows a circuit for SWR mode support. It features two capacitors, C3017 and C3018, connected to PIN23 and ground. C3017 is labeled 4.7U/6.3V/X5R and C3018 is labeled 0.1U/16V_4. The capacitors are connected in parallel between PIN23 and ground.

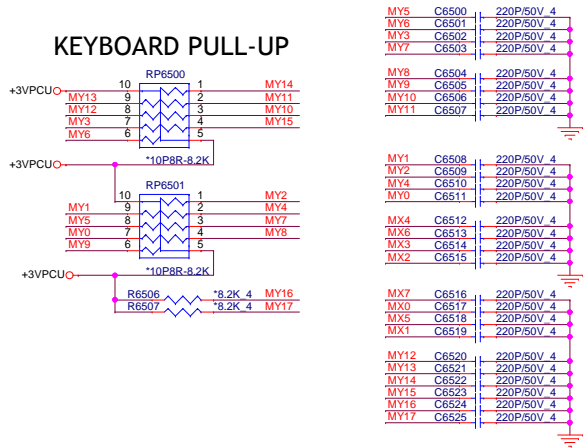




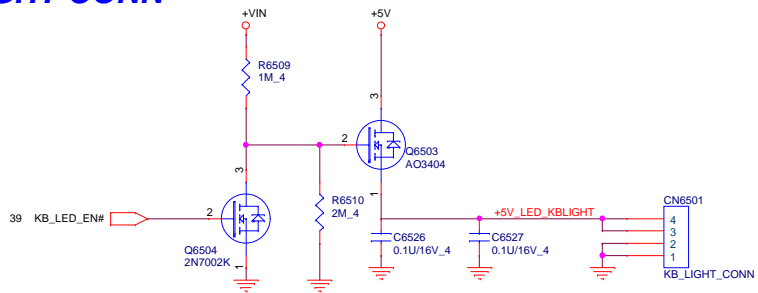
KEYBOARD Con.



KEYBOARD PULL-UP



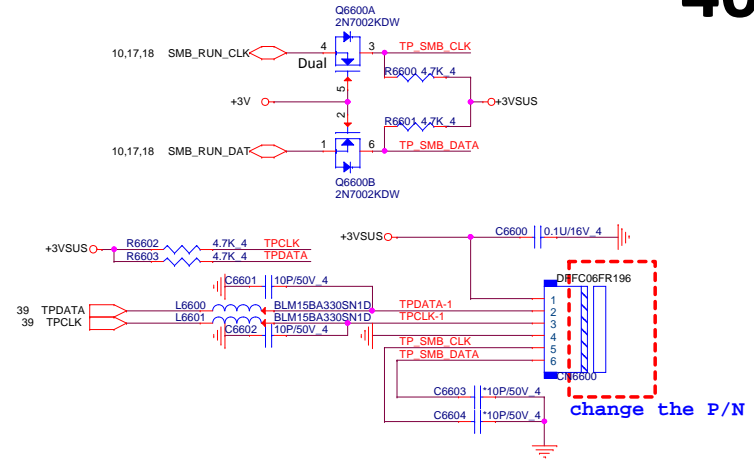
KB LIGHT CONN



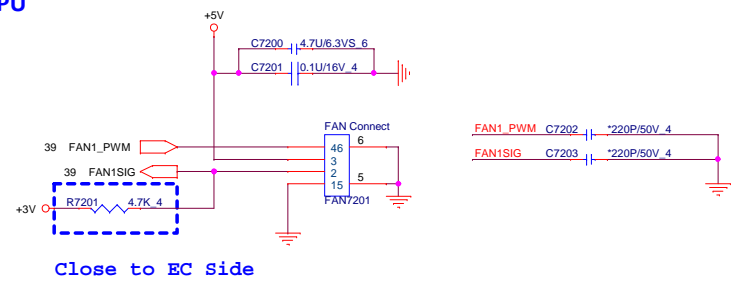
Quanta_Confidential

Touch Pad Connector

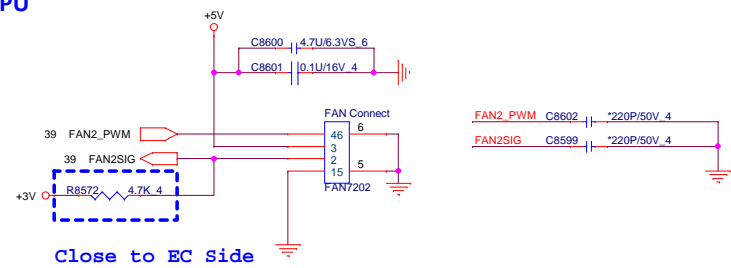
40

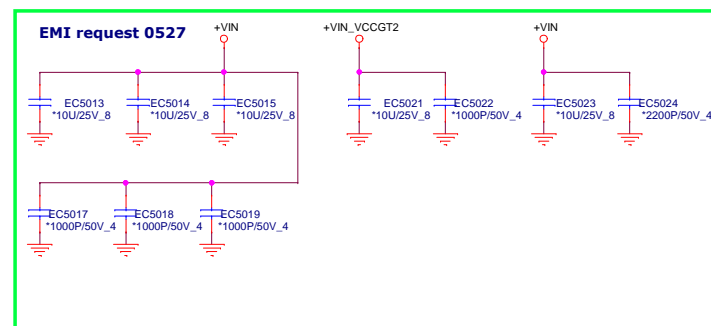
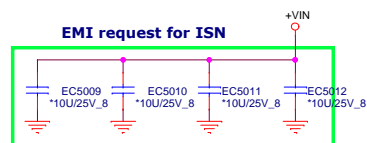
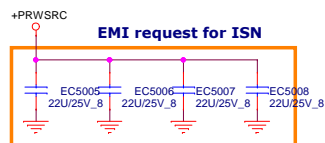


FAN1 for CPU

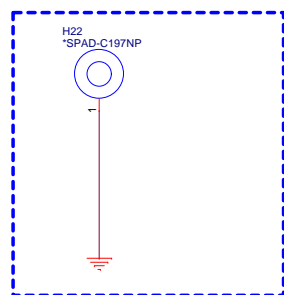


FAN2 for GPU

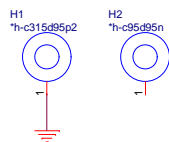




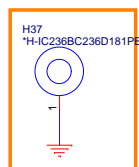
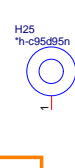
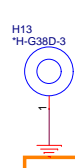
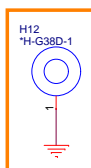
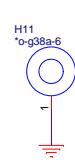
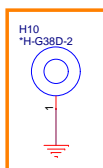
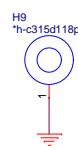
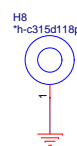
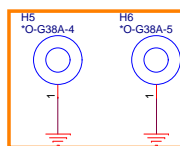
HOLE



Place to TOP(EMI)

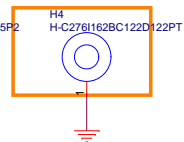


SI change

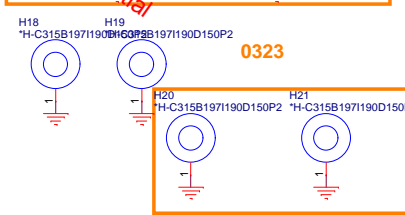
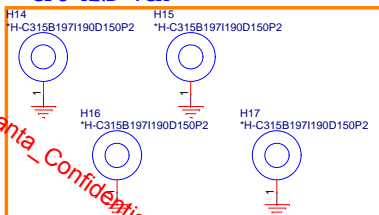


0322

WLAN NUT on BOT



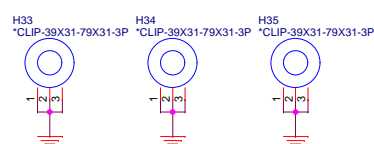
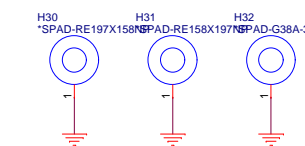
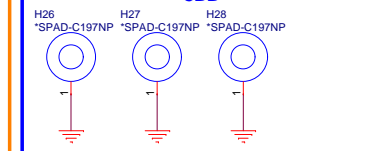
CPU AND VGA



PCH NUT on BOT



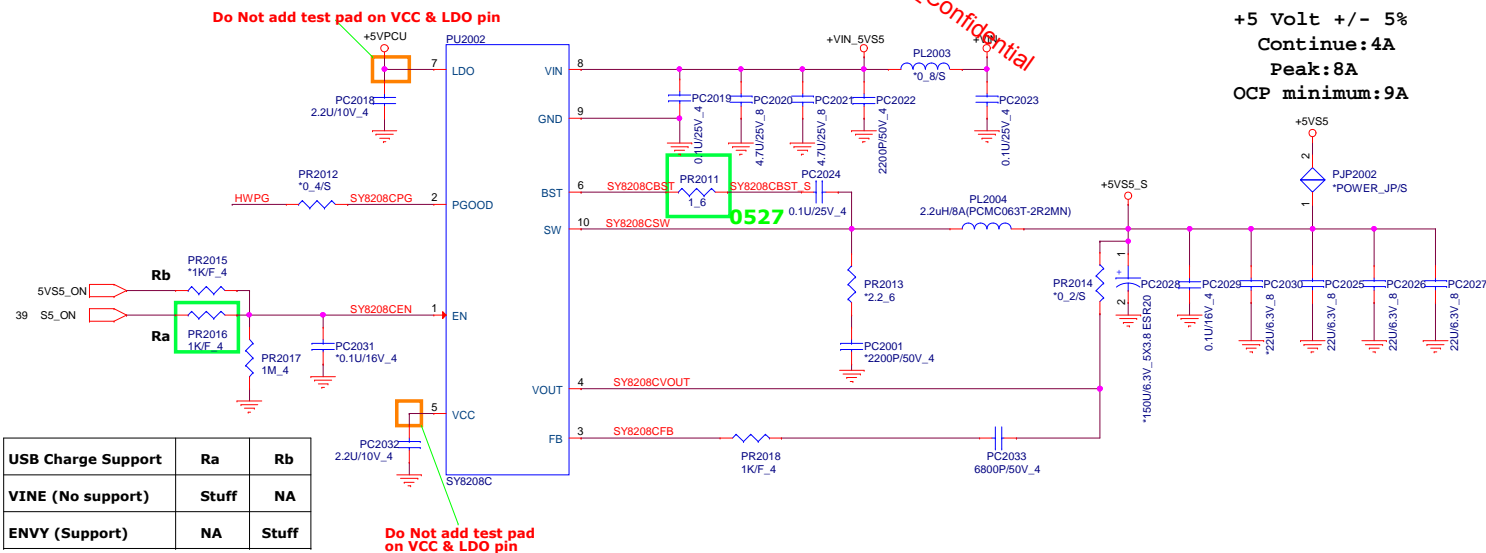
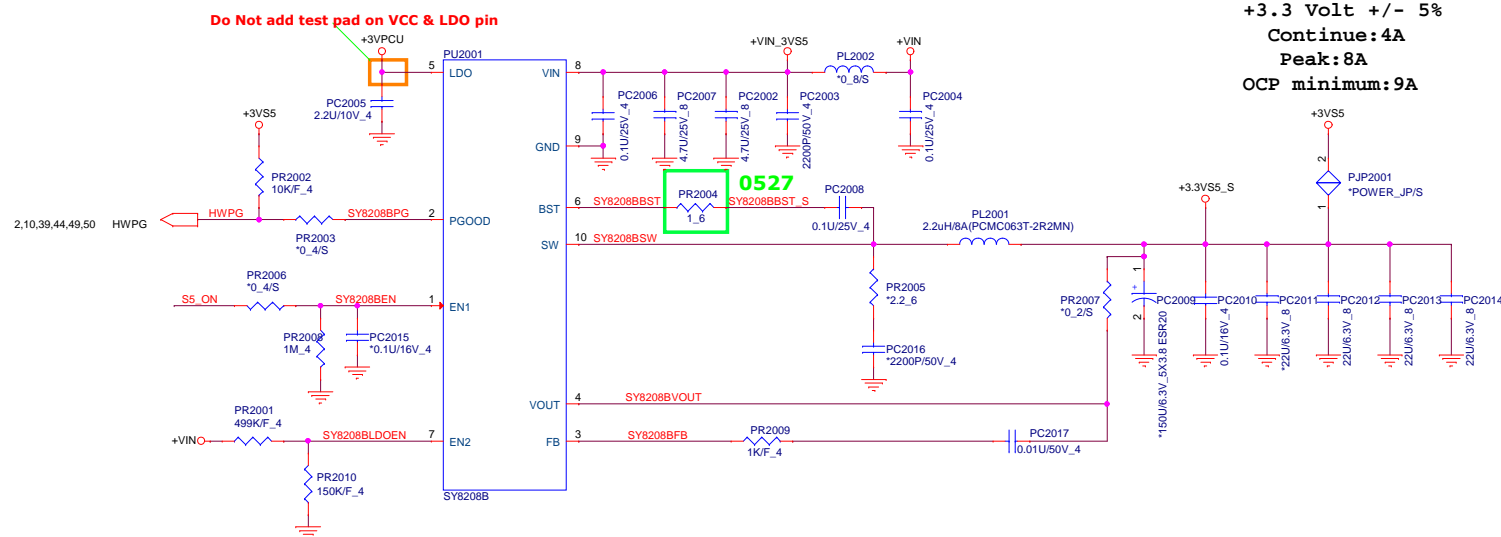
ODD



PROJECT : G38A
Quanta Computer Inc.

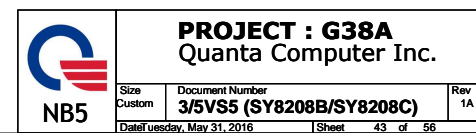
Size	Document Number	Rev
Custom	RF Solution/HOLE	1A
Date: Wednesday, June 01, 2016	Sheet 41 of 56	

2xxx

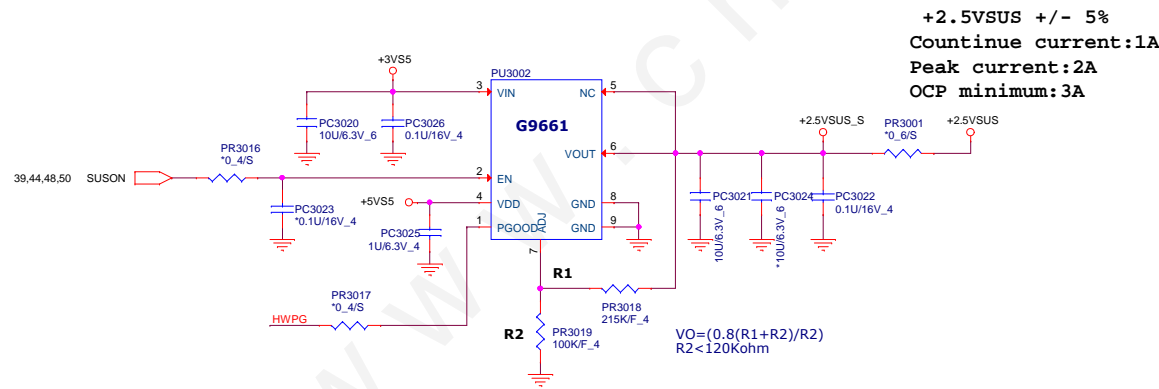
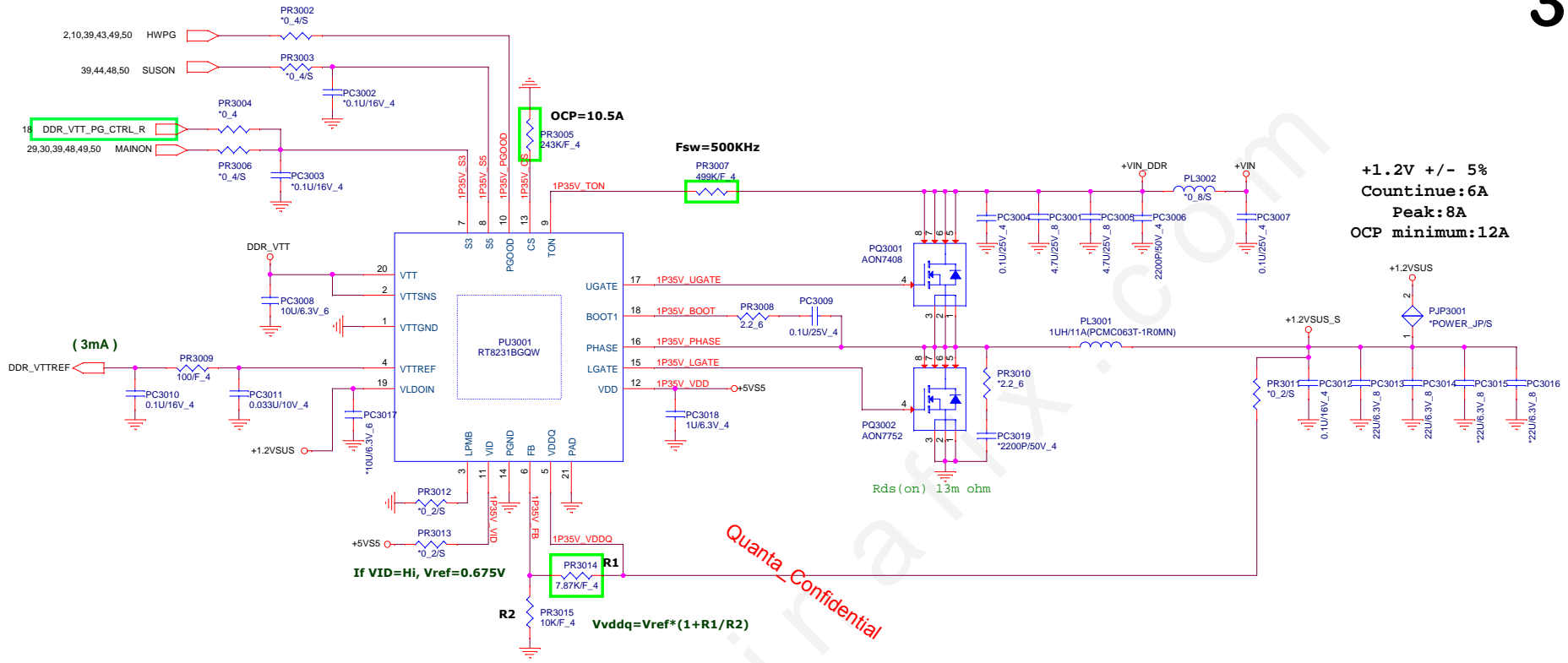


USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

+VIN	28,40,41,42,44,45,46,47,48,49,50,51,54
+3VS5	10,12,14,16,28,29,30,35,39,44,48,49,50
+5VS5	10,28,31,33,44,45,46,47,48,49,50,51,52,53,54,55
+3VPCU	5,10,21,33,35,39,40,42,51
+5VPCU	31,42,48,55



3xxx



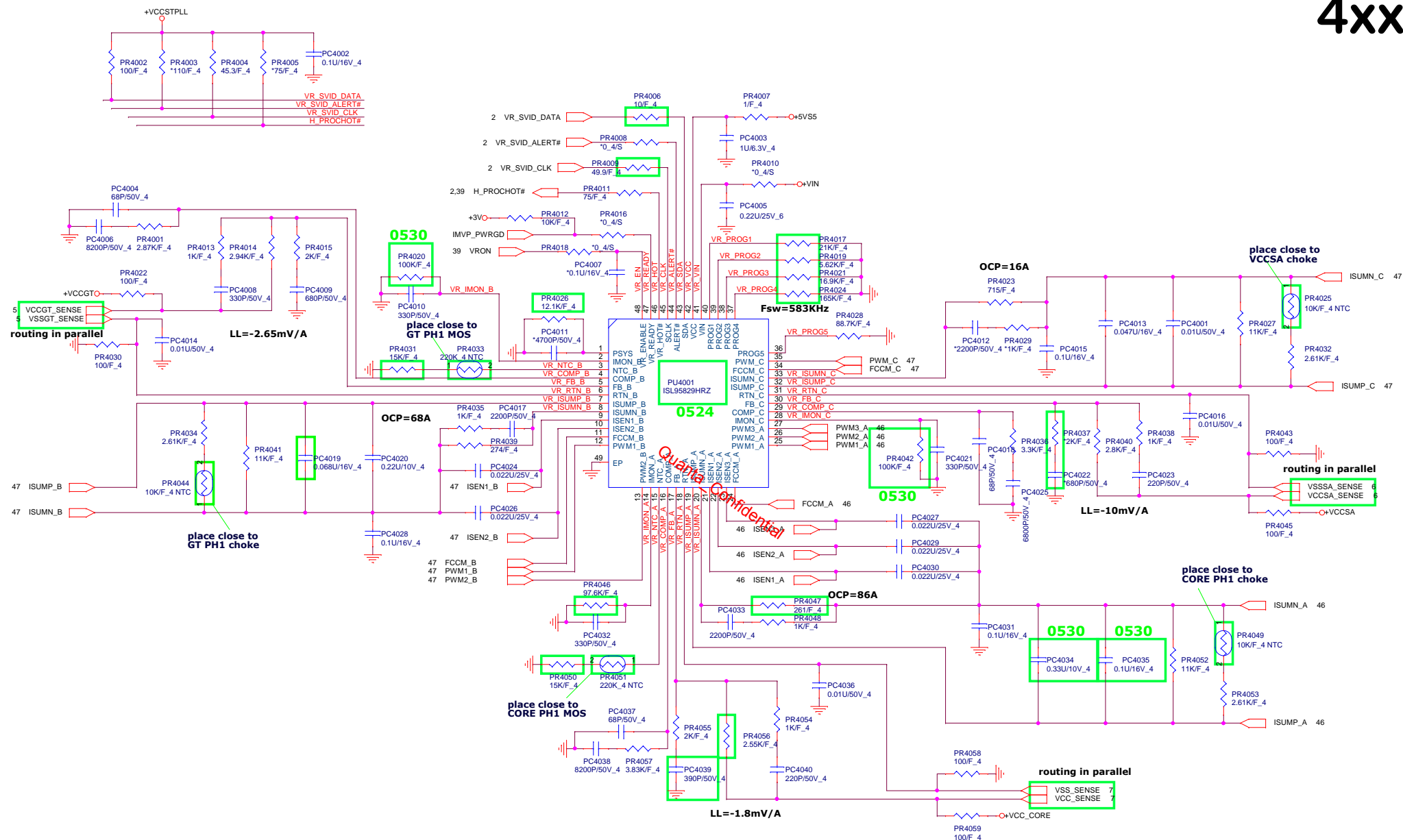
+VIN	28,40,41,42,43,45,46,47,48,49,50,51,54
+5VS5	10,28,31,33,43,45,46,47,48,49,50,51,52,53,54,55
+1.2VSUS	2,6,10,17,18,50,55
DDR_VTT	17,18
+2.5VSUS	17,18

	PROJECT : G38A Quanta Computer Inc.		
	Size	Document Number DDR3 (RT8231B)	Rev 1A

Tuesday, 02/01/2016

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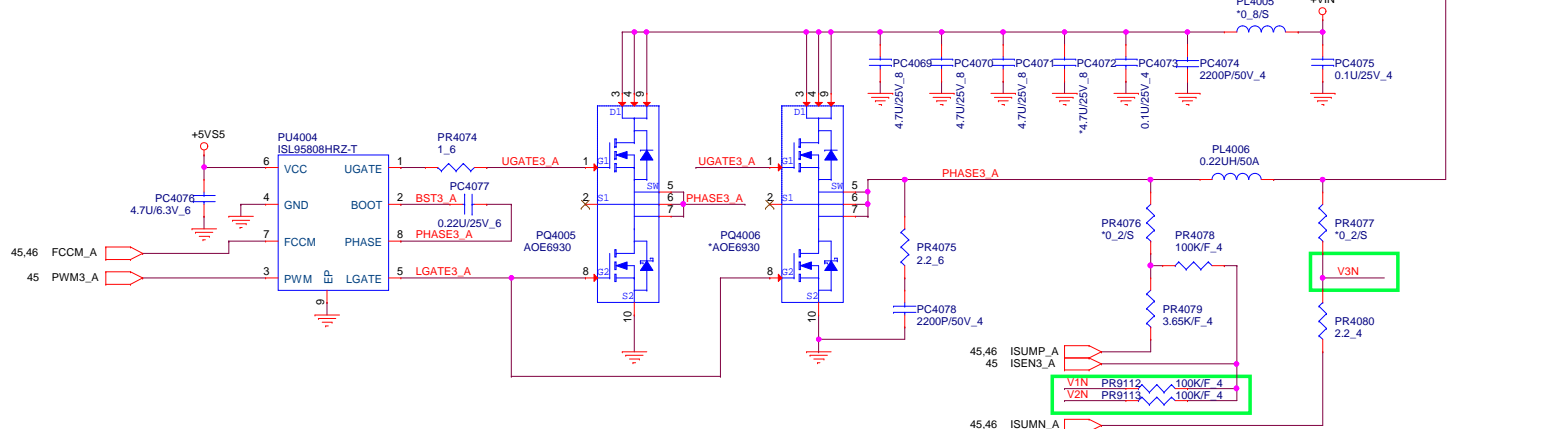
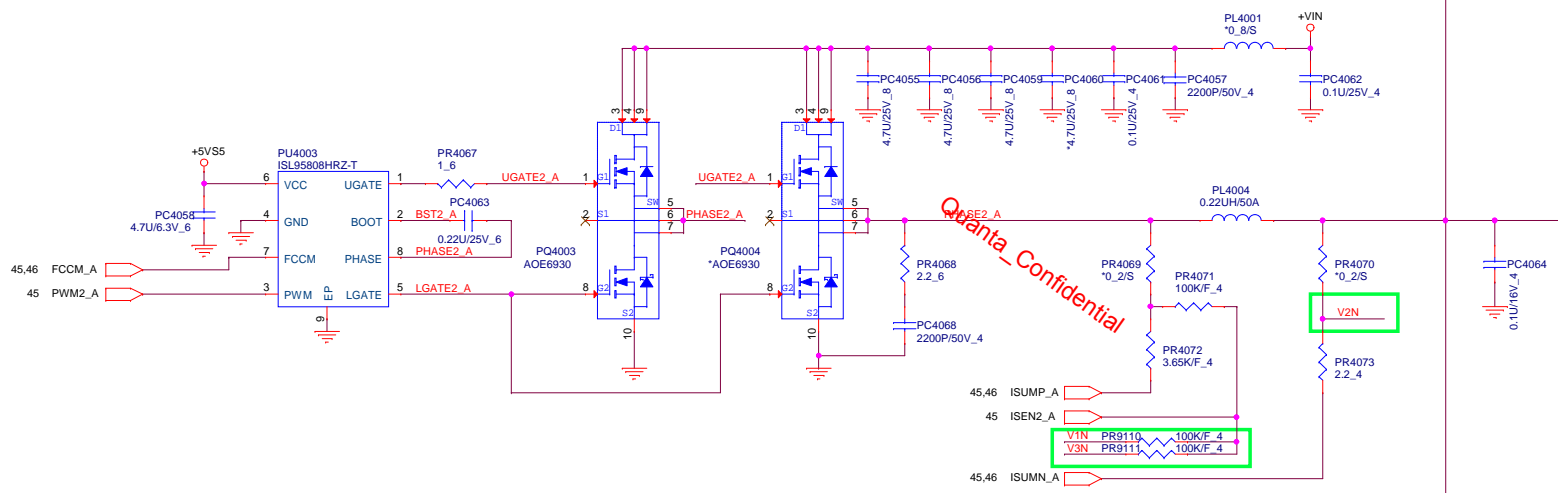
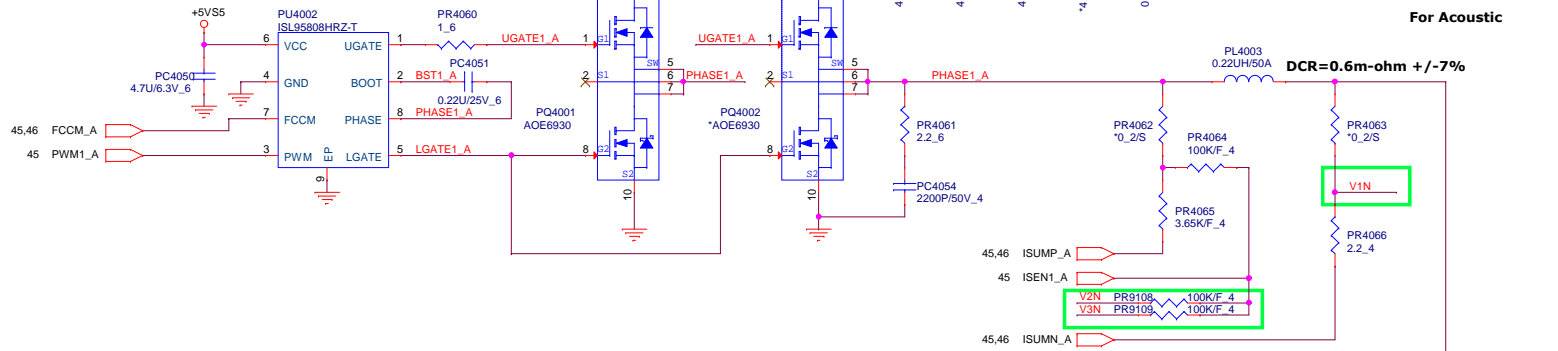
4xxx



PROJECT : G38A
Quanta Computer Inc.

Size Custom	Document Number CPU VR IC (ISL95829HRZ)	Rev 1A
Date: Tuesday, May 31, 2016		Sheet 45 of 56

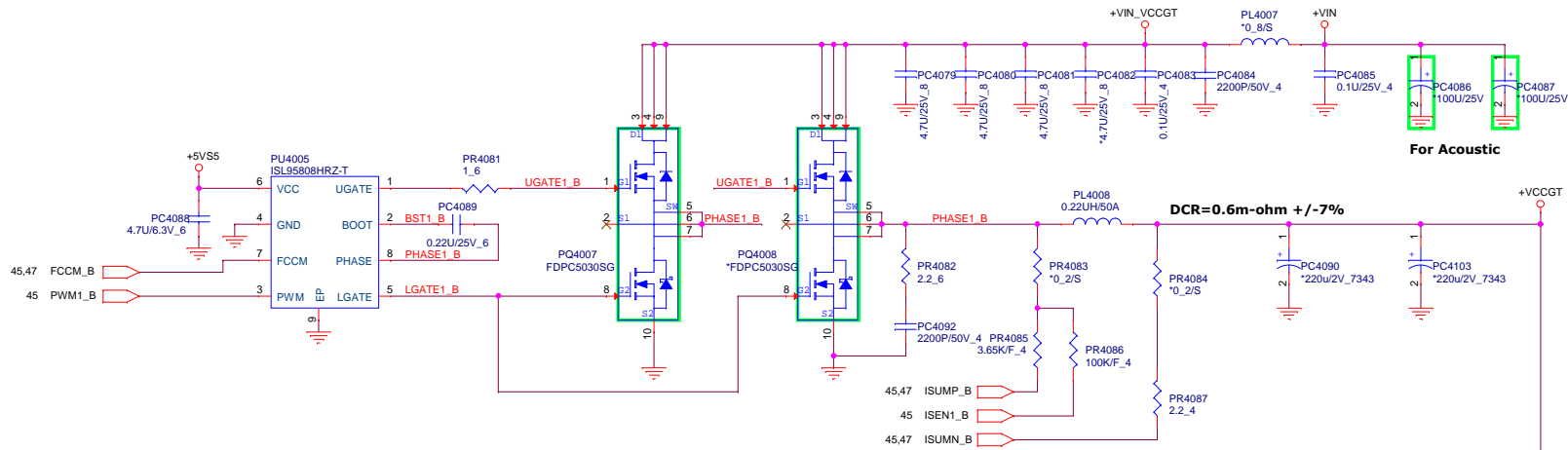
4xxx



H-line42(35W)
TDC:44A
Iccmax:60A
OCP:86A
Loadline = -1.8 mV/A

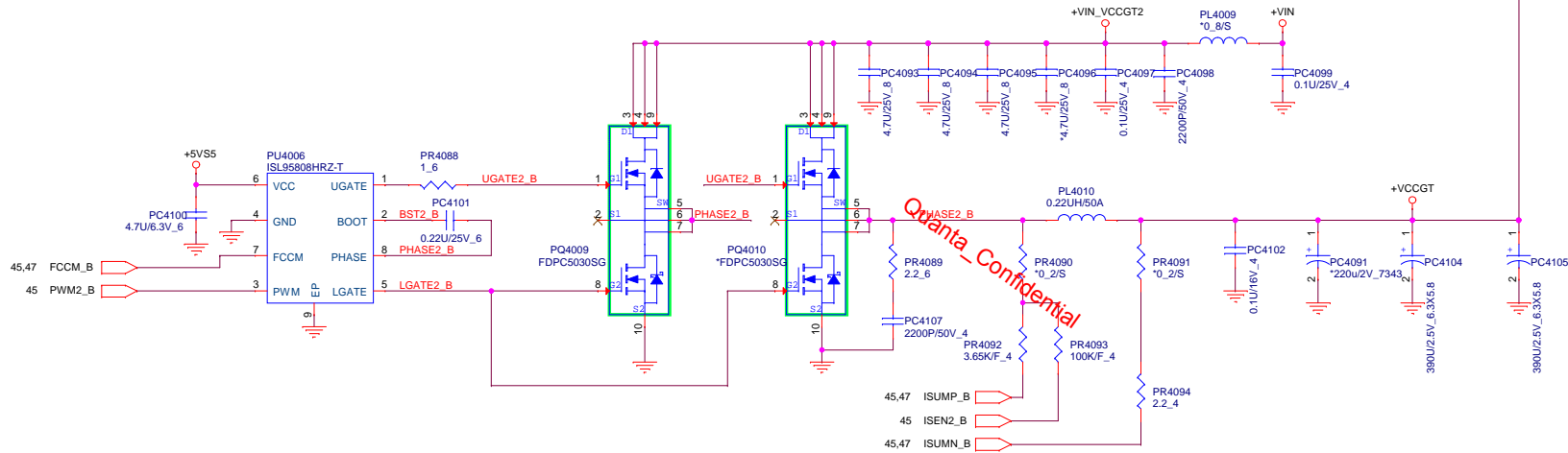
H-line42(45W)
TDC:50A
Iccmax:68A
OCP:86A
Loadline = -1.8 mV/A

4xxx

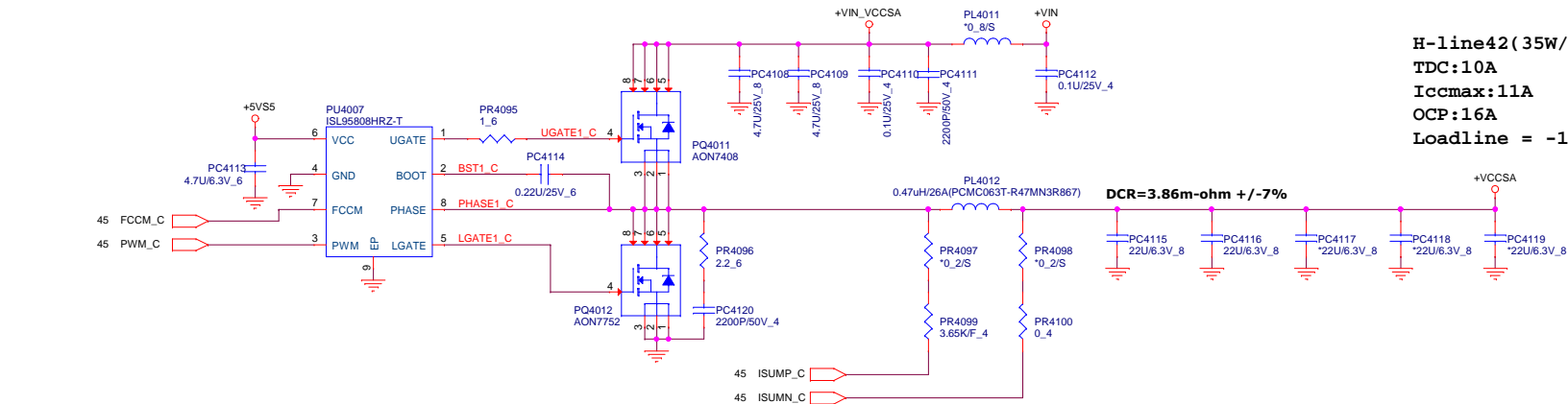


H-line42 (35W)
TDC:25A
Iccmax:55A
OCP:68A
Loadline = -2.65 mV/A

H-line42 (45W)
TDC:25A
Iccmax:55A
OCP:68A
Loadline = -2.65 mV/A

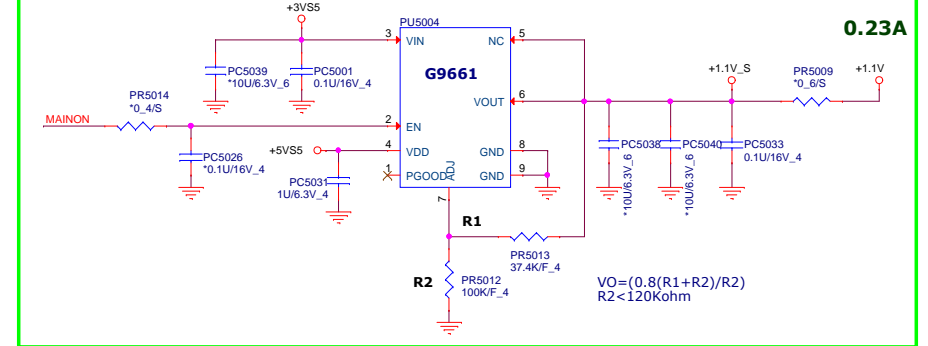
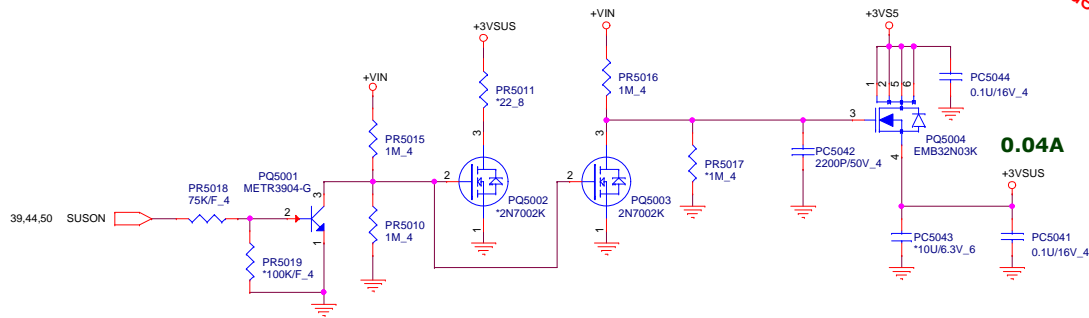
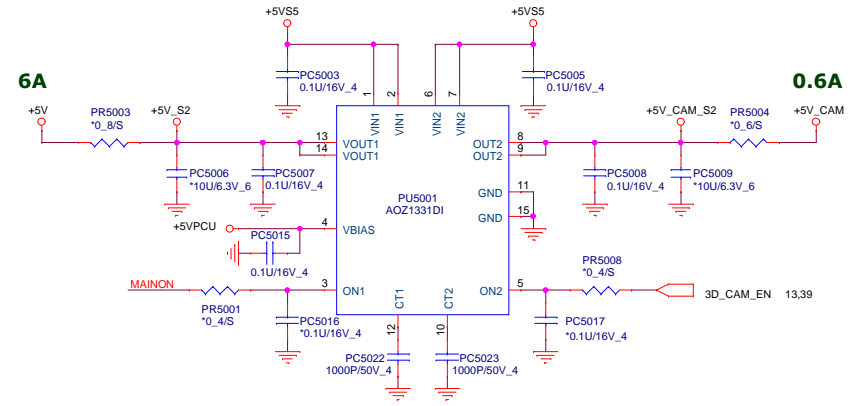
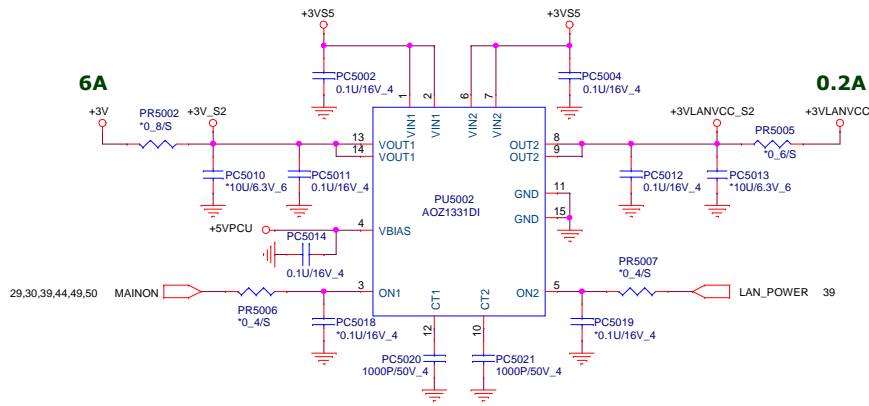


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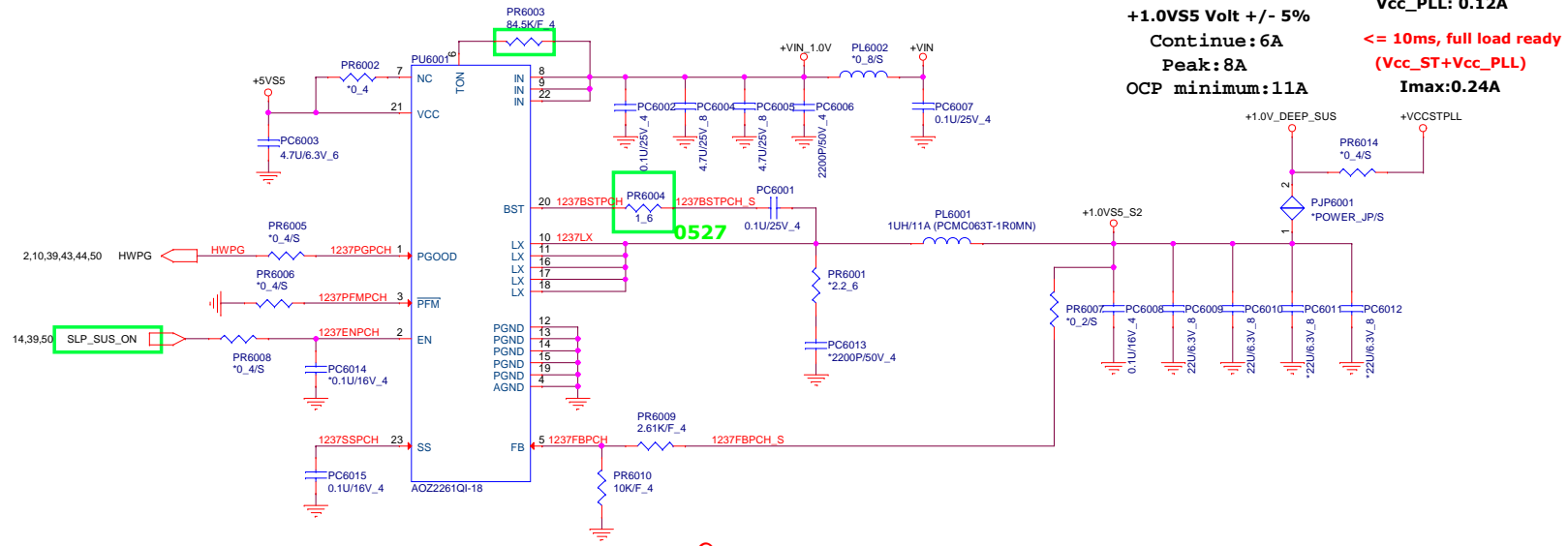


H-line42 (35W/45W)
TDC:10A
Iccmax:11A
OCP:16A
Loadline = -10 mV/A

5xxx



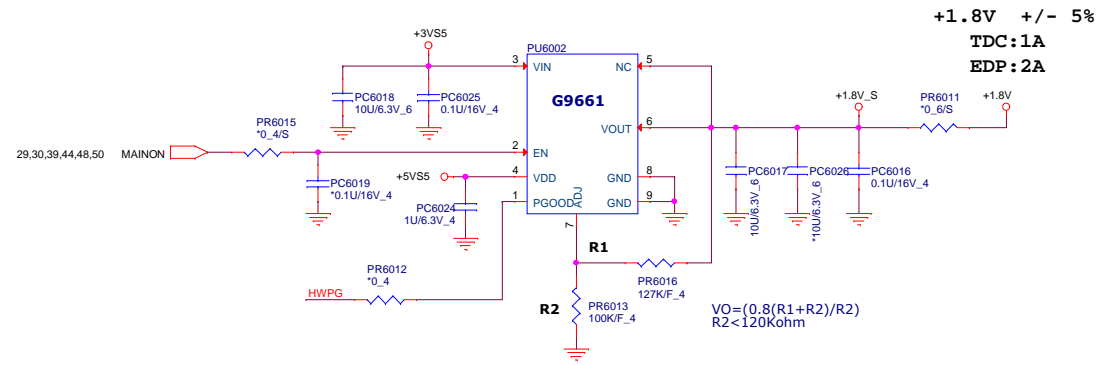
- +3V 5,9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,34,35,36,37,38,39,40,45,54,55
- +5V 28,29,31,32,34,40
- +3V_S5 10,12,14,16,28,29,30,35,39,43,44,49,50
- +5V_S5 10,28,31,33,43,44,45,46,47,49,50,51,52,53,54,55
- +3V_SUS 40
- +3VLAVCC 37
- +5V_CAM 34



(V1.00A+V1.00_MODPHY+VccPRIM_CORE)
+1.0V55 Volt +/- 5%
 Continue: 6A
 Peak: 8A
 OCP minimum: 11A


Volume Segment
 Vcc_ST: 0.12A
 Vcc_PLL: 0.12A
 <= 10ms, full load ready
 (Vcc_ST+Vcc_PLL)
 I_{max}: 0.24A

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+1.8V +/- 5%
 TDC: 1A
 EDP: 2A

- +VIN 28,40,41,42,43,44,45,46,47,48,50,51,54
- +3VS5 10,12,14,16,28,29,30,35,39,43,44,48,50
- +5VS5 10,28,31,33,43,44,45,46,47,48,50,51,52,53,54,55
- +1.0V_DEEP_SUS 10,11,14,50
- +1.8V 22,31,32,33,34,55
- +VCCSTPLL 2,6,45
- +1.1V 29,48



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Size Custom	Document Number +1.0_DEEP_SUS	Rev 1A
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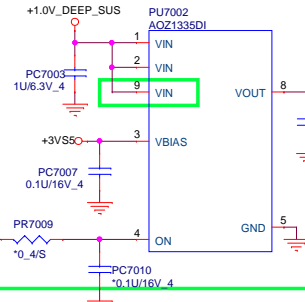
7xxx

Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 5.5A

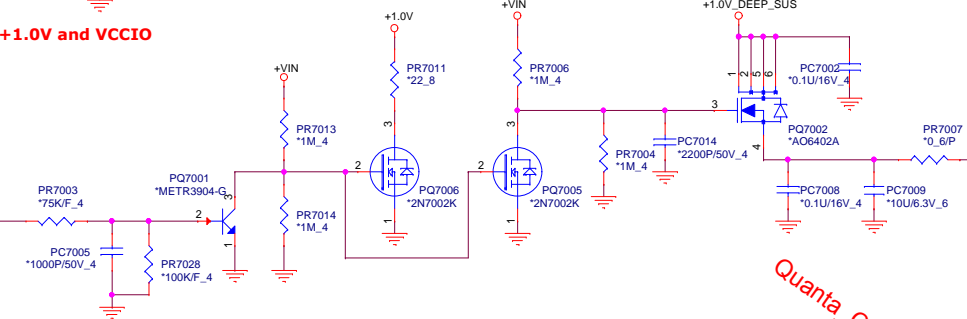
<= 10ms full load ready

Imax:5.5A

Imax:0.04A

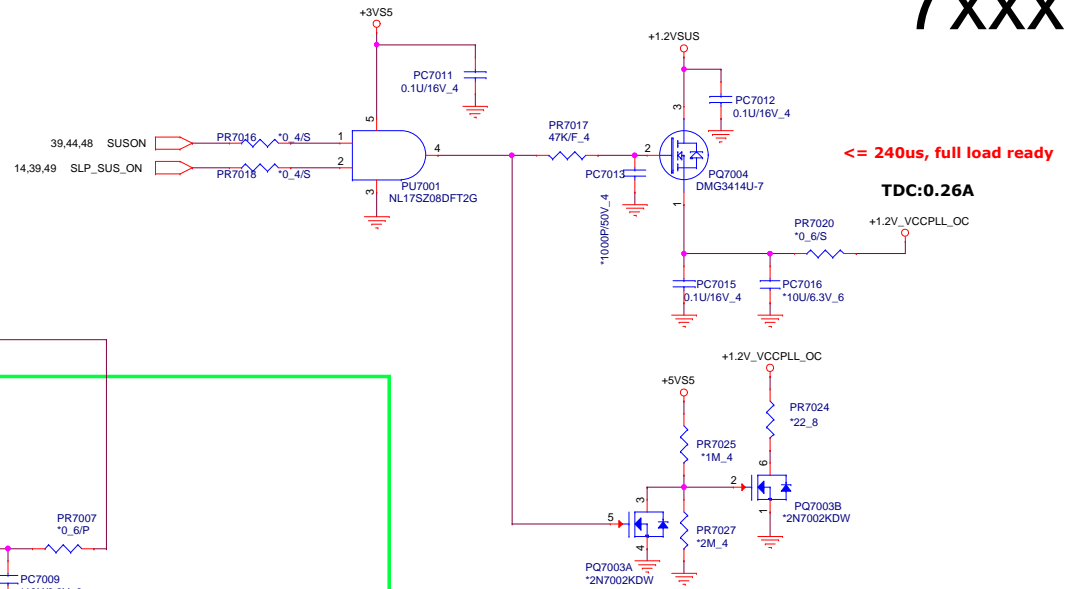
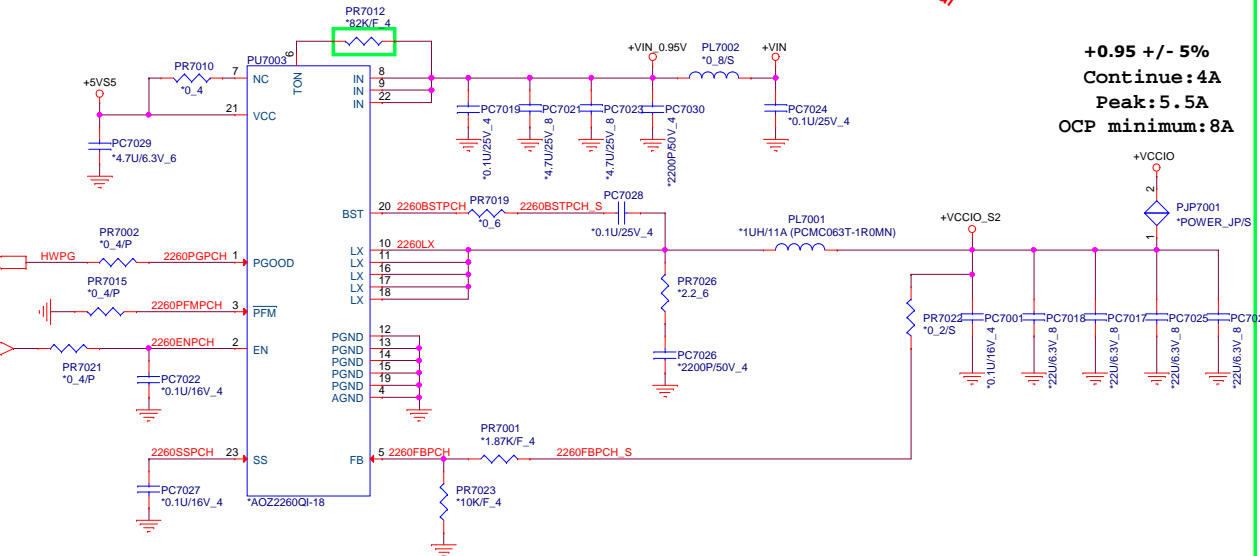


Reserve for separating +1.0V and VCCIO



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+0.95 +/- 5%
Continue:4A
Peak: 5.5A
OCP minimum: 8A



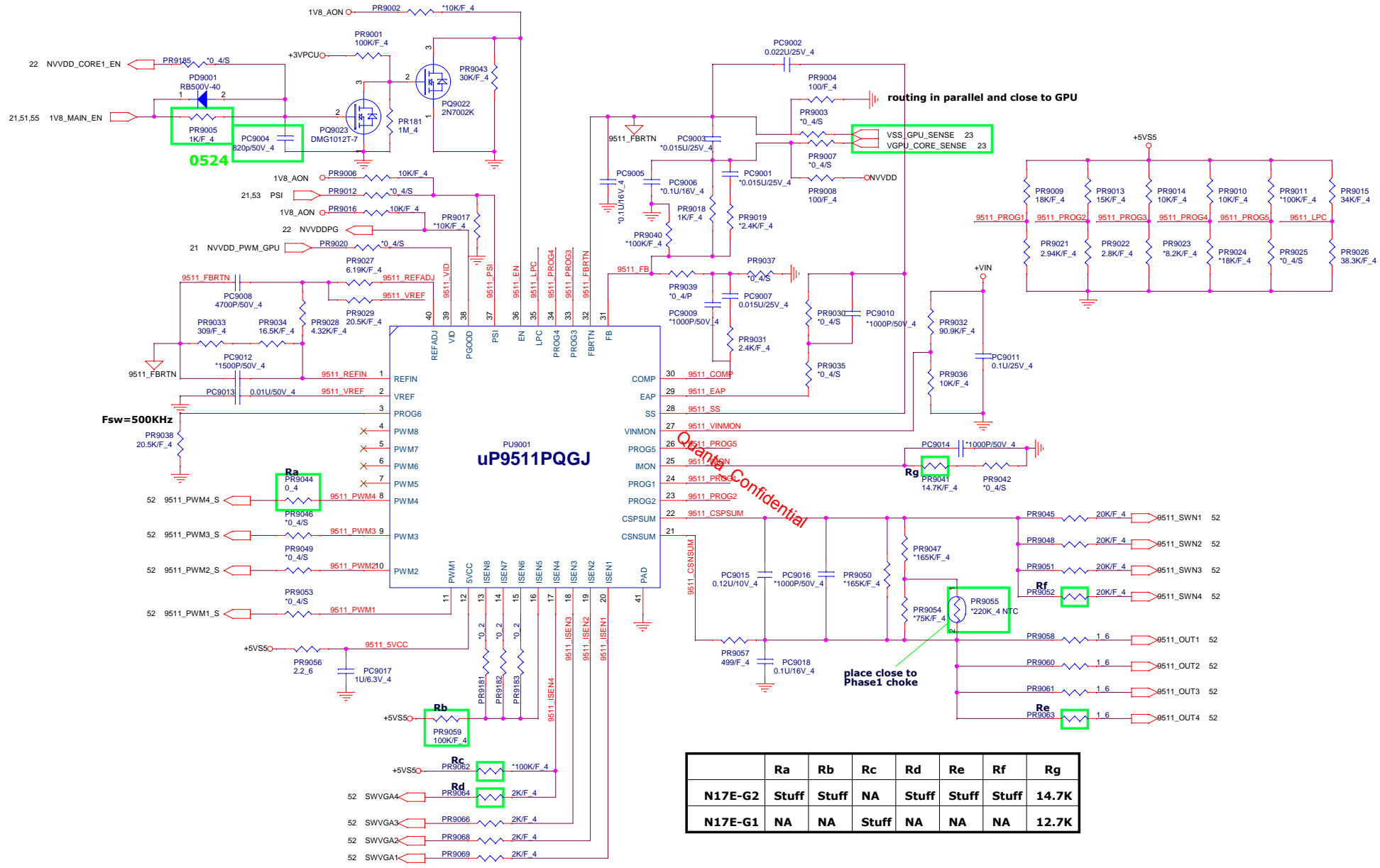
<= 240us, full load ready

TDC:0.26A

- +1.0V 2,5,6,10,39
- +3VS5 10,12,14,16,28,29,30,35,39,43,44,48,49
- +5VS5 10,28,31,33,43,44,45,46,47,48,49,51,52,53,54,55
- +VCCIO 3,6
- +1.0V_DEEP_SUS 10,11,14,49
- +1.2VSUS 2,6,10,17,18,44,55


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	Ra	Rb	Rc	Rd	Re	Rf	Rg
N17E-G2	Stuff	Stuff	NA	Stuff	Stuff	Stuff	14.7K
N17E-G1	NA	NA	Stuff	NA	NA	NA	12.7K

- +3V 5,9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,34,35,36,37,38,39,40,45,48,54,55
- +VIN 28,40,41,42,43,44,45,46,47,48,49,50,54
- +5VS5 10,28,31,33,43,44,45,46,47,48,49,50,52,53,54,55
- 1V8_AON 19,21,22,53,54,55
- NVDD 23,52
- 1V8_MAIN_EN 21,51,55



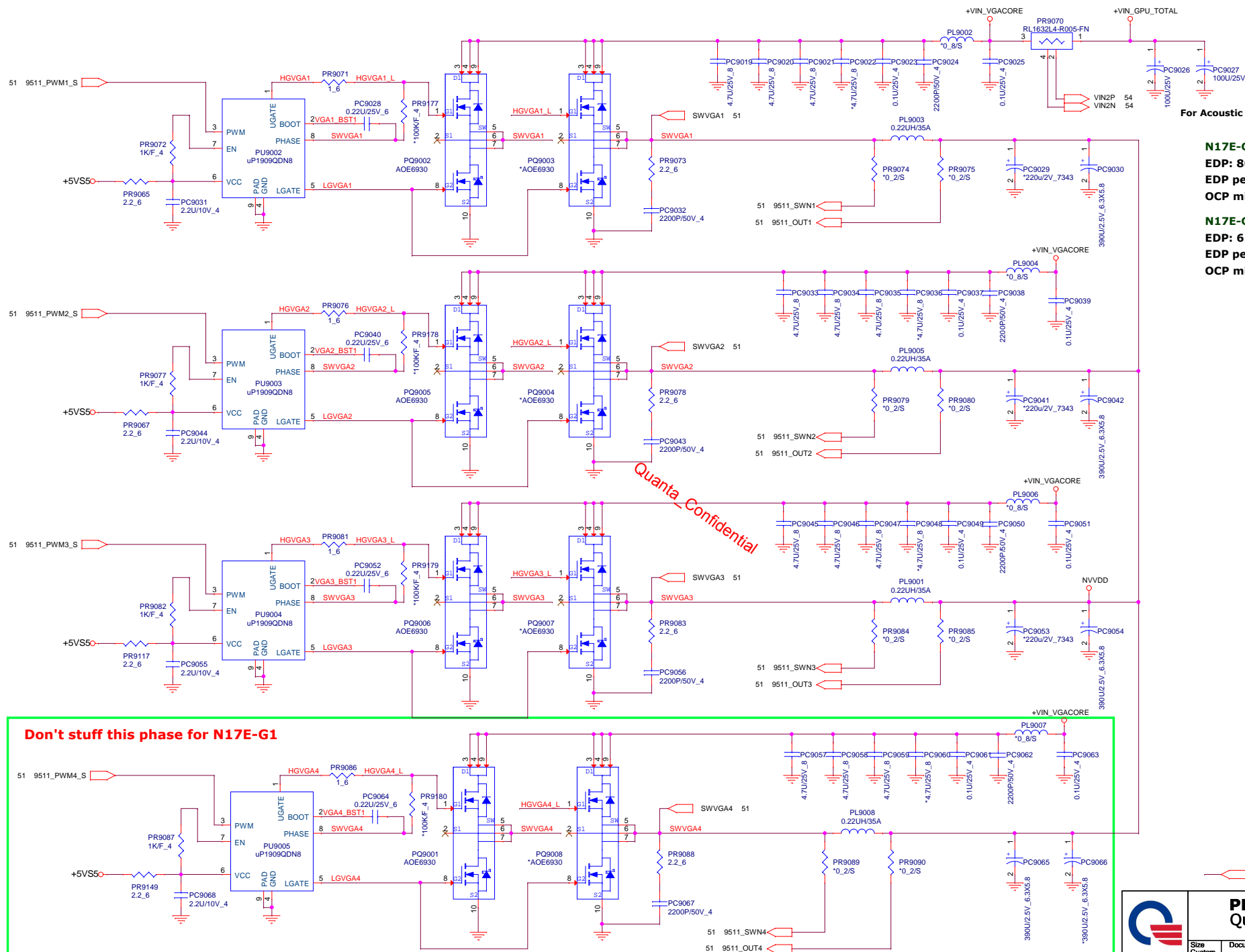
PROJECT : G38A
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For Acoustic

N17E-G2 (82W)
EDP: 80A
EDP peak: 204A
OCP minimum 245A

N17E-G1 (65W)
EDP: 62A
EDP peak: 164A
OCP minimum 197A



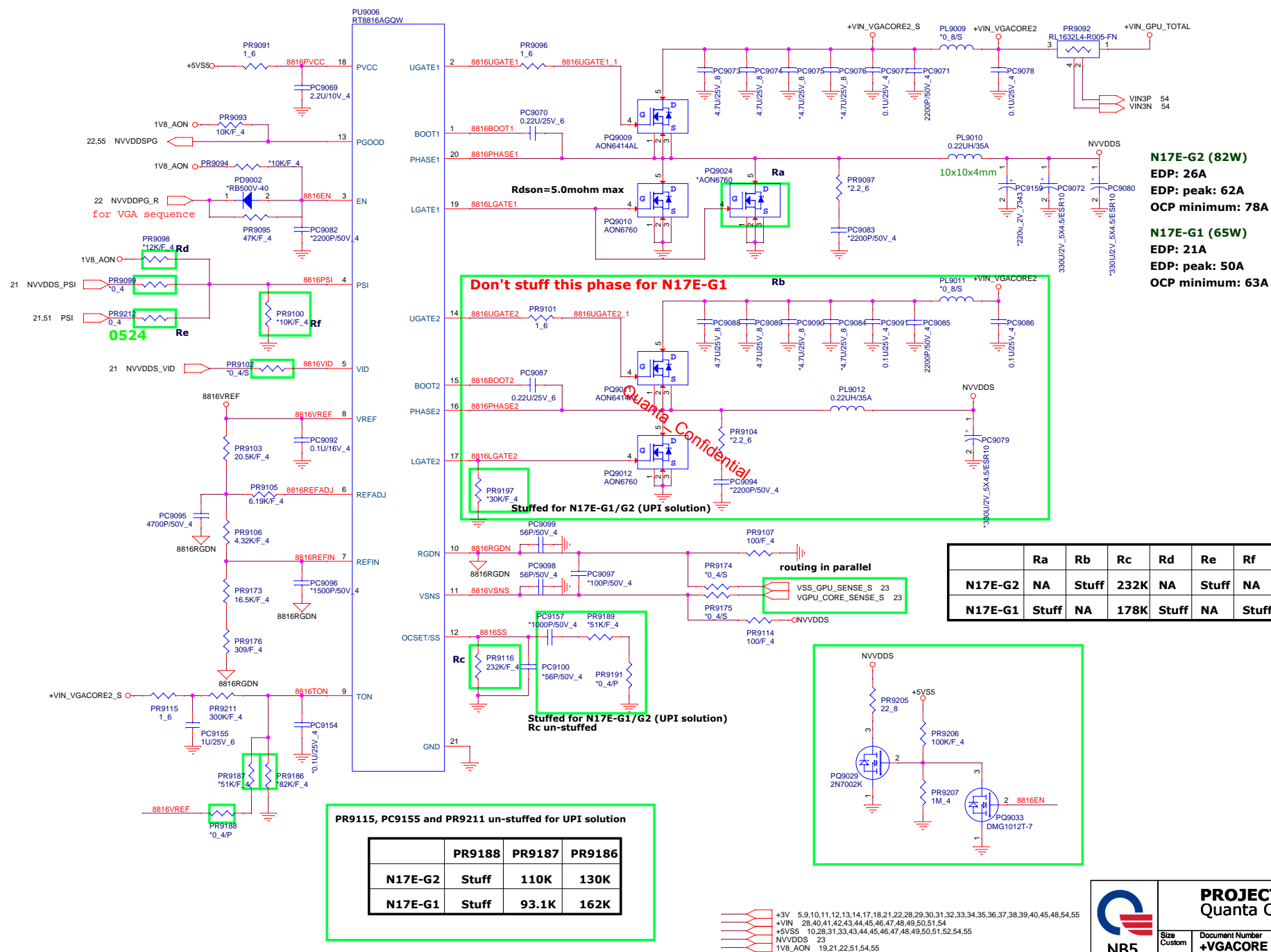
 NVVDD 23,51



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9xxx



9xxx

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.55V/1.5V
0	1.35V

FBVDDQ_MEM	R1	R2
1.55V	35.7K	53.6K
1.5V	30.9K	69.8K

PR9142, PC9156 and PR9145 un-stuffed for UPI solution

	PR9196	PR9195	PR9194
N17E-G2	Stuff	93.1K	162K
N17E-G1	Stuff	93.1K	162K

1.35V/1.55V +/- 5%
N17E-G2 (82W)
EDP: 29A
EDP: peak: 53A
OCF minimum: 64A

N17E-G1 (65W)
EDP: 25.2A
EDP: peak: 46A
OCF minimum: 64A

Stuffed for N17E-G1/G2 (UPI solution)


Stuffed for N17E-G1/G2 (UPI solution)
 PR9147 un-stuffed



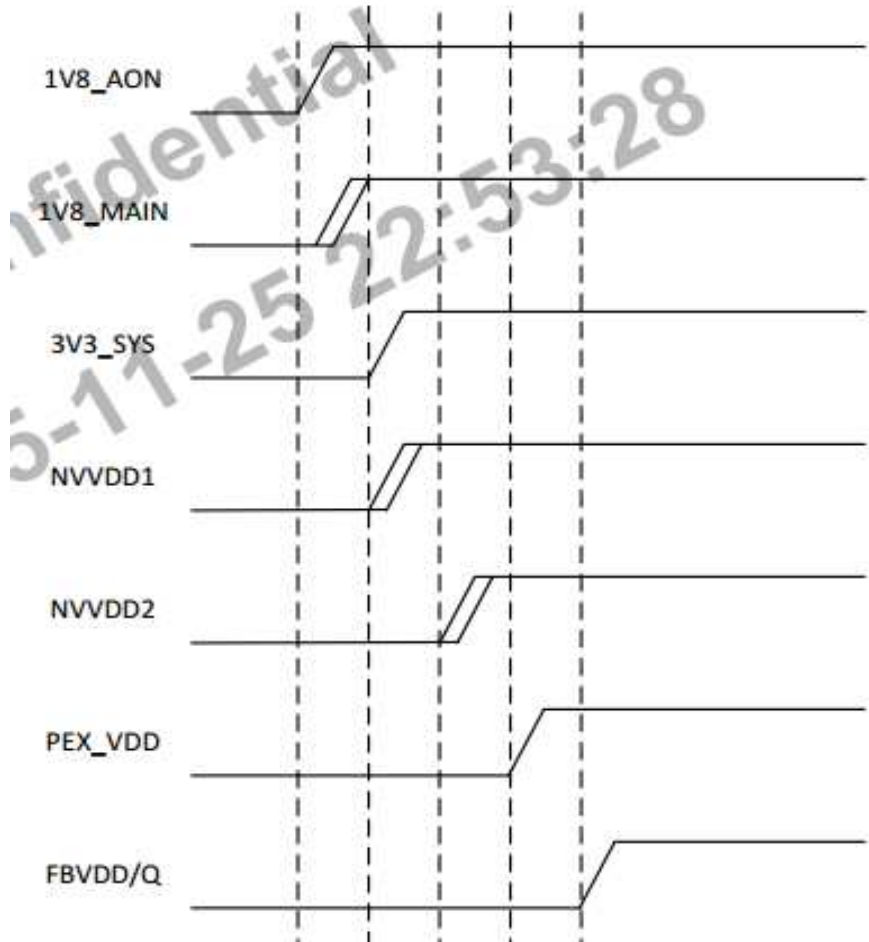
PROJECT : G38A
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.35V_GFX (AOZ2263QI-18)	1A
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The schematic diagram shows the internal structure of the PU9009 AOZ1331DI converter. The input voltage is 1V8_MAIN, and the output voltage is 1V8_AON_S. The input current is 0.9A, and the output current is 1.0A. The circuit includes a feedback network with resistors PR9158, PR9159, PR9160, and PR9161. The output is connected to a load resistor PR9161. The circuit is labeled with component values and pin numbers.

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	Size Custom	Document Number +3V/+1.05V_GFX(AOZ1331DI)	Rev 1A
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N17E-G2 Power on sequence



N17E-G2 Power off sequence

NVVDDS--->PEX--->NVVDD/FBVDDQ
----->1V8_MAIN----->1V8_AON

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